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ENGINEERING SERVICES ON
TRANSISTORS

REPORT NO. 8

THIRD QUARTERLY PROGRESS REPORT

PERIOD COVERED: 1 JANUARY TO 31 MARCH 1962
DATE OF THIS REPORT: 31 MAY 1962

Contract DA 36-039 sc-88931
(Continuation of Contract DA 36-039 sc-88962)
File No. 00523-PM-62-91-91 (4905)
DA Project No. 3A-99-21-001

U. S. Army Signal Research and Development Laboratory
Fort Monmouth, N. J.

Prepared by Bell Telephone Laboratories, Incorporated
On behalf of Western Electric Company, Incorporated
222 Broadway, New York 38, N. Y.

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DA Project No. 3A-99-21-001
Signal Corps Technical Requirements No. SCL-7570, 20 September 1960
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U.S. Army Signal Research and Development Laboratory
Fort Monmouth, N. J.

OBJECT

The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices, together with their circuit properties and applications, with a view toward demonstrating and increasing the practicability of their use in operating equipment.

This report was prepared by Bell Telephone Laboratories, Incorporated
On behalf of Western Electric Company Incorporated
222 Broadway, New York 38, N. Y.

The following engineers and scientists participated in its preparation:

R. E. Davis	B. T. Howard	D. A. Naymik
A. G. Foyt	R. Lindner	G. Reich

SUMMARY OF STATUS

Work on this contract is a continuation of that carried out on Contracts Da 36-039 sc-88962, DA 36-039 sc-85352 and earlier contracts of this continuous series.

Status of Tasks 4 and 9 is summarized below. Tasks 1, 2, 3, 5, 6 and 8 have been completed as reported previously under earlier contracts. Task 7 is inactive by mutual agreement. A final report is being prepared on Task 2.

During the period covered by this report, 1 January to 31 March 1962, approximately 2000 engineering man-hours were devoted to work on this contract.

This contract was terminated as of 31 March 1962 but the work will be continued on a new contract, DA 36-039 sc-89201.

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Work has continued on the development of the microwave transistor, M2275, and the 1-watt, 1000-mc transistor, M2260. Planar structures, using oxide separation between the emitter and base electrodes, are being used for both transistor types.

Evaporation jigs have produced structures within the tolerance limits allowed in the initial design. Processing problems which are associated with the evaporation of the oxides, have limited the fabrication of the devices. Scattering of the oxide during evaporation has been the chief problem, and many of the scattering sources have been eliminated. M2260 structures have been made which show transistor action with a current gain of 8, but further process development is necessary before satisfactory devices can be made in a highly reproducible manner.

Designs for a new power header for the M2260 are being investigated so that the requirement of very low header parasitic impedances can be met. Prototypes of a new design have been assembled and they show significantly lower input and output inductance than the previous coaxial header. A technique for determining the temperature rise in the new designs has been worked out.

Characterization and design studies have been continued to provide additional information which is necessary to optimize the structure of both devices.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Studies to evaluate alternative methods of integrating circuits and subsystems functions are continuing. These studies indicate that the specific technique of integration, i.e., multiple-like device packaging, functional packaging, or hybrid packaging required to optimize a given subsystem function is determined by the circuit construction of the particular function.

Work has continued on technique studies of integrating a twenty-four bit register. The results of these studies show that significant savings in the number of cans, external leads and number of boards can be obtained using presently available technology. Even greater gains appear to be achievable with more advanced technology.

A system clock, designed to provide sixteen output pulses, spaced at an interval of one millisecond has been built using integrated circuit techniques. Circuit tests have been completed and show that the clock is operating in the prescribed manner.

Work is continuing on the development of technology related to integrated circuits.

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LIST OF ILLUSTRATIONS

SECTION 1 - PURPOSE

The general purpose of this contract is to make studies and investigations related to transistors and transistor-like devices, together with their circuit properties and applications, with a view toward demonstrating and increasing the practicality of their use in operating equipment. This contract is a successor to preceding contracts of a similar nature: Contract W36-039 sc-44497, Contract DA 36-039 sc-5589, Contract DA 36-039 sc-64618, Contract DA 36-039 sc-85352, and Contract DA 36-039 sc-88962.

These contracts call for services, facilities, and material to be employed on mutually acceptable tasks. Of the nine tasks assigned, five have been completed with final reports. Work on Task 2, Transistor Reliability was terminated in August 1961. A final report is being prepared. Brief descriptions of other tasks and dates of Final Reports are contained in Section 1 of Report No. 6 dated 31 December 1961, the First Quarterly Report issued under the present contract.

Tasks currently active under this contract are outlined below.

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

The contractor shall make theoretical and experimental studies leading to exploratory models and, upon mutual agreement, to feasibility designs of:

1. New transistors using new or previously untried principles.
2. New transistors obtained by studied modifications of existing types.

The new transistors shall be primarily intended and suitable for application to voltage, current, and power amplifiers, and to associated electronic transducers.

In general, transistors having ac amplifying properties in the following ranges are of particular interest:

1. Germanium transistors from 1000 mcps to 3000 mcps with as large power ratings as the state of the art permits.
2. Silicon transistors from 100 mcps to 1000 mcps with as large power ratings and as high temperature ratings as the state of the art permits.
3. Devices of other materials with specific attention to obtaining frequency, power, noise, or temperature advantages over germanium and silicon devices.

TASK 4A - MICROWAVE TRANSISTOR

The Contractor shall conduct a study and investigation leading to the design and fabrication of a transistor capable of operating with a minimum of 10-db gain at 3000 mc. The transistor structure should be of a diffused base mesa type with stripe emitter and base electrodes or with dot emitter and ring base electrodes. An accurate design theory for such a device shall be established together with an appropriate equivalent circuit including package parameters. It is desired that the transistor be matched into 50-ohm input and output coaxial terminations. From a microwave point of view the structure (package and transistor) shall be basically broadband. Ideally, the transistor should be capable of greater than 10-db power gain from d.c. to 3000 mc. Appropriate experimental models of such devices including any necessary adapters, indicative of the progress made shall be furnished during the course of this program.

TASK 4B - 1000 MC, 1 WATT TRANSISTOR

The Contractor shall conduct a study and investigation leading to the design and fabrication of a transistor capable of operating with a minimum of 1 watt of power output at 1000 mc with a minimum gain of 10 db and with a minimum efficiency of 30 per cent, for this power output and gain. An accurate design theory for such a device shall be established together with an appropriate equivalent circuit including package parameters. The structure shall be an hermetically sealed package with provisions for mounting on simple heat sinks. Appropriate experimental models of such devices, including any necessary adapters, indicative of the progress made shall be furnished during the course of this program.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

The Contractor shall make theoretical and experimental studies leading to exploratory models, and upon mutual agreement, to feasibility designs and finally to development models of semiconductor components able to perform more complex functions than existing components can, thereby reducing the number of components needed in electronic systems with the ultimate objective of improving the reliability and reducing the cost of such systems. The components to be investigated shall include:

1. Functional devices, namely devices designed from physical phenomena to perform as directly as possible desired systems functions.

2. Diodes and transistors in miniature insulated packages to be compatible with thin film resistor-capacitor techniques. These packages may form an integral part of an insulating substrate on which resistive and capacitive films may be evaporated to form complete circuits.

3. Integrated circuits, namely combination of circuit elements including, where appropriate, functional devices designed and fabricated as units to perform desired systems functions.

The work shall include but not be limited to:

1. Evaluation of systems requirements and related components requirements with attention to such figures of merit as speed, gain, power dissipation, impedance,

reliability, packing density, interconnection topology, etc. A study shall be undertaken of selected categories of semiconductor components to determine their universality with respect to a variety of systems. For example, integrated diode-transistor logic circuits shall be studied for gating and flip-flop circuits. The gating circuits studied shall be designed for optimum fan-in, fan-out requirements. The fan-in, fan-out requirements should be based upon systems analysis.

2. Study of miniature diodes and transistors in insulated packages shall be undertaken to determine the effects, if any, of the packaging techniques on the performance and reliability of these devices. Wherever possible, comparative conventional devices shall be used to make this analysis most meaningful.

3. Fabrication of these selected exploratory components and circuits to determine their figures of merit. For example, four-layer, three-terminal device structures (PNPN) having turn-off gain properties shall be investigated for application to functional circuits. In addition, the contractor shall endeavor to determine the reliability inter-relationship of several semiconductor devices (i.e. diodes and transistors) contained in a common sealed package or several junctions fabricated in a common semiconductor wafer.

4. The cost factors associated with all of the above shall be investigated, particularly with respect to yield on multiple devices in common package or multiple junctions within one wafer.

SECTION 2 - ABSTRACT

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Chapter 1 reports the status of the M2275 microwave transistor. Fabrication of devices has been limited by difficulty in production of the oxide rings of the desired quality necessary to make the proposed planar structure. Scattering of the oxide during evaporation proves to be the chief source of trouble. A systematic study of the problem has been made and the quality of the oxide deposits has been improved. Noise figure calculations for the device have been made as a function of base resistance, and a noise figure of less than 5 db at 1000 mc appears reasonable with terminations consistent with adequate amplifier gain and stability.

The status of the M2260, 1-watt, 1-kmc transistor is reported in Chapter 2. Work during this interval has been concentrated on the fabrication of the oxide-spaced structure. The modified evaporation jig has consistently produced evaporated structures within the tolerance limits allowed in the initial design, and results to date show the possibility of reducing the tolerance limits from + 1 mil to ± 0.2 mil. This reduction of the tolerance limits would increase the stability and bandwidth of the unit by decreasing stray capacities. The scattering of SiO during evaporation has been decreased but not eliminated. Many of the units made during this quarter show emitter-to-base shorts, and it has not been determined whether this is caused by pinholes in the oxide, or by surface alloying under the oxide. Units without shorts have shown transistor action with a common-emitter current gain of 8.

Mesa units have been used for characterization during this interval since no completed oxide-spaced units have been available. High frequency y-parameter measurements were taken for three 3-stripe mesa units with 1 x 20 mil stripes. All of these units exhibited an abnormally high value of g_{22} at 1 kmc and above, giving a unilateral gain at 1 kmc of approximately 2 db. An explanation of this effect, consistent with the measurements, has been derived by considering the resistance in series with that part of the collector capacity which is not directly under one of the base electrodes. The calculation of this series resistance from measurements and calculated equivalent circuit element values, gives a value consistent with the mesa border and base doping.

The design for a new M2260 header is discussed, including preliminary electrical measurements, and the calculation of its thermal properties.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

A study of the effect of the use of different classes of integrated circuit packages on circuit board layout is presented in Chapter 3. In particular a number of subsys-

tem functions are examined so that a comparison can be made of the layouts resulting from the use of integrated circuit packages containing multiple-like devices, logic gates or hybrid arrangements. The optimum circumstances are defined as those which lead to a minimization of the size of the layout, the number of package codes, the total number of packages and the number of leads. It is found, with the use of these criteria, that the packaging technique used should be flexible enough to permit any or all classes of integrated circuit packages to be fabricated if layout optimization is required.

Chapter 4 extends the earlier study by considering the effect of evolving technology on the integrated circuit packages which could be used to construct a 24-bit register. Four variations in the type of integration to be used are considered. The studies show that the basic concept of integrating through the use of multiple-device chips in a single encapsulation is compatible with an evolving program to develop integrated circuit technology.

Chapter 5 presents a simple reduction to practice of the concept developed in the earlier chapters. The subsystem function chosen to be implemented was a system clock consisting of a multivibrator, four binary counters and sixteen logic gates. Integration was carried out through the use of multiple-semiconductor-device chips in a single encapsulation. The integrated clock possessed the same characteristics as an unintegrated version and has been operated for about one-hundred hours without difficulty.

SECTION 3 - PUBLICATIONS AND REPORTS

During the period covered by this report, no publications or other reports were issued.

SECTION 4 - FACTUAL DATA

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Chapter 1

STATUS OF THE M2275 TRANSISTOR

By A. G. Foyt

1.1 INTRODUCTION

The M2275 is to be a p-n-p germanium diffused-base transistor with circular emitter and base contacts and a planar collector-base junction. The collector-base junction is defined by an oxide ring and the emitter and base contacts are separated by a second oxide ring. The transistor is designed for use as a common-base tuned amplifier in the low microwave frequency range. A diagram of the transistor wafer is shown in Fig. 1. The device design and structure have been discussed more fully in the two previous quarterly reports (Refs. 1, 2).

During this quarter the principal effort has been directed toward process development for the fabrication of the structure. Many of the process steps for this device, diffusion, electrode evaporation, and alloying are similar to those used in the mesa structure and have not presented difficulty. The deposition of the oxide rings for the collector diffusion mask and for separation of the base and emitter electrodes requires refined evaporation techniques. Early oxide evaporation runs did not provide sharp, well-defined edges on the rings and the scattering of the oxide into the emitter and base electrode regions subsequently hindered alloying of the electrodes. A systematic study of factors influencing edge definition of the rings and scattering of the oxide has been carried out. As a result the appearance of the rings has been improved to the point where they should be satisfactory for transistor fabrication.

Also, during this quarter, the noise performance of the proposed transistor has been studied using an equivalent circuit for the transistor and a noise figure computed from the equivalent circuit. The calculations show a noise figure of less than 5 db at 1 Gc for the proposed transistor. Minimum noise figures of approximately 2 db are calculated, but in a useful amplifier circuit they will not be obtainable since they require a source impedance which is not consistent with adequate gain and stability.

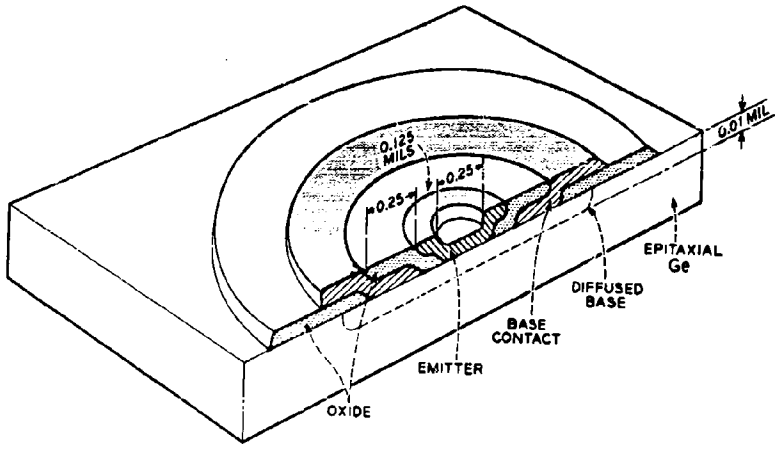


Fig. 1 - M2275 oxide-separated structure

1.2 PROCESSING

The area of processing which has presented new problems which were not previously encountered in mesa transistor fabrication is associated with the deposition of the oxide rings. The sequence of process steps in which the oxide deposition is involved are the following:

(1) Evaporation of the outer oxide ring on the germanium slab.

(2) Removal of the germanium from the evaporation jig.

(3) Diffusion of the base layer.

(4) Realignment of the wafer in the evaporation jig.

(5) Evaporation of the base contact ring.

(6) Evaporation of the inner oxide ring.

(7) Evaporation of the emitter electrode.

(8) Alloying.

Steps 3, 5, 7 and 8 follow mesa-transistor technology and have not required additional work. The problem of realigning the wafer in the evaporation jig after base-layer diffusion and the evaporation of the emitter and base electrodes was discussed in the previous quarterly report (Ref. 2). Using the present evaporation tool, realignment of the germanium wafer with the evaporation mask is satisfactory for fabrication of this transistor. The evaporation and alloying of the emitter and base contacts and the diffusion of the base layer seem to be satisfactory for transistor fabrication.

The evaporation of the inner and outer oxide rings have presented the greatest fabrication problem during this quarter. The oxide scatters over the germanium surface during evaporation. This scattered oxide prevents alloying of the emitter and base contacts to the germanium. This problem may be avoided either by reducing the amount of scatter during evaporation, or by chemical removal of the thin

scattered oxide from the germanium after evaporation. The germanium can be cleaned easily after evaporation of the outer oxide ring and before base-layer diffusion to remove scatter from the evaporation. However, a similar cleaning after evaporation of the inner oxide ring does not seem desirable for two reasons. First, a chemical treatment would remove part of the base layer and would possibly increase base resistance. Secondly, the realignment of the germanium wafer for evaporation of the emitter would require a second difficult realignment step in the processing and increase the danger of low yield.

Because the chemical cleaning of the germanium does not appear desirable after evaporation of the inner oxide ring, the evaporation techniques were studied in an attempt to understand and reduce the oxide scatter. This study of evaporation techniques is described in the following section.

1.3 DEVELOPMENT OF OXIDE EVAPORATION

To achieve the dimensions shown in Fig. 1, without chemical cleaning of the oxide rings, every evaporated ring must be confined to the size shown in the figure with a minimum of scattered material outside the allowed area. In particular, the scatter from the outer oxide ring must be no greater than about 0.1 mil if the base ring is to contact the germanium. As noted previously, in some initial attempts to make this transistor, the oxide scatter prevented alloying of the emitter and base contacts.

In order to study the oxide scatter, some measure of scatter must be defined. The test used for this study was a functional test of gold alloyed to germanium. That is, a thin layer of gold was evaporated over the oxide and germanium wafer, and the wafer was heated to the gold-germanium eutectic temperature. The area which alloyed was said to be sufficiently free of scattered oxide.

Using this test, a series of experiments was performed to evaluate the effects of evaporation procedure on the formation of clean, well defined, oxide deposits. Figs. 3, 4 and 5 show some evaporation results using various evaporation methods. The results of these experiments are discussed below.

1.3.1 Evaporation Source

It was found necessary to use a small effective source diameter to obtain well defined edges on the deposits. To do this, a cap with a 0.1-inch hole was placed over the evaporation source as shown in Fig. 2. However, there was evidence of evaporation, probably due to surface migration of oxide on the cap, from the upper surface of the cap. To eliminate the effect of this evaporation, the source was redefined by two shields, each with 0.125 inch holes, placed immediately above the source as shown in Fig. 2. There was no evidence of evaporation from the upper surface of the top shield, so that the effective source size was about 0.125 inches.

1.3.2 Shielding Between Source and Germanium

It was found that any shielding, such as shields 3 and 4 in Fig. 2, between the effective source and the germanium provides a surface for scattering of the evaporated oxide, and may increase the amount of scattered oxide on the germanium.

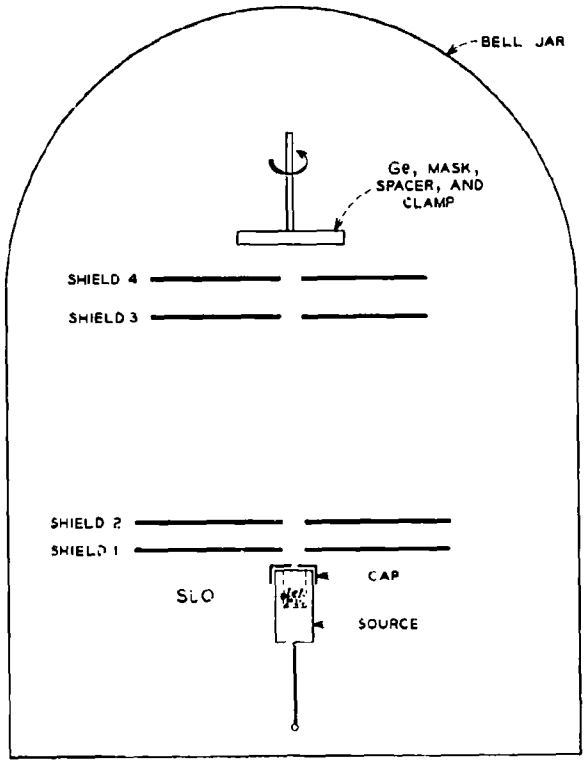


Fig. 2 - Cross section of evaporator

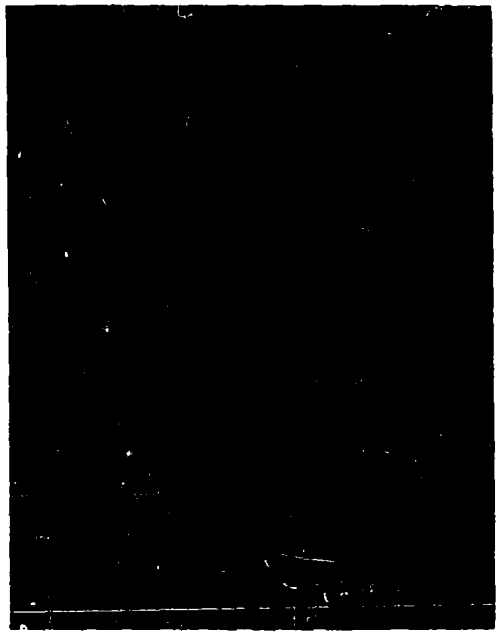


Fig. 3 - Oxide evaporation, initial results. Shields 3 and 4, 1-inch holes; shield 2 removed; shield 1, 1/4-inch hole. Ge heated to 300°C, ring of oxide evaporated, and sample covered with gold. Photo shows a typical evaporated ring (dark ring) surrounded by scattered oxide (lighter rectangle). No alloying was seen in this sample.

For this reason, no shielding was placed between the effective source and the germanium for the best evaporation results.

1.3.3 Germanium, Evaporation Mask, and Clamp Assembly

A reduction of the temperature of the germanium, mask, and clamp assembly caused a reduction in the amount of scattered oxide. The mask and clamp assembly do provide potential sources of scatter, and further work is necessary to determine the effect of this assembly on the oxide scatter.

Using the techniques discussed above, the oxide dots shown in Fig. 5 were evaporated on a germanium surface. Similar dots, when covered with the amount of gold that will be used in the transistor, showed alloying up to the edge of the dot. This evaporation result is of device quality and this evaporation procedure will be used in the transistor fabrication.

1.4 CALCULATION OF NOISE FIGURE

There has been interest shown in the noise performance of this proposed transistor in the Gc frequency range, especially at 1 Gc. To evaluate the noise performance, a noise figure F will be calculated for the proposed transistor at 1 Gc.

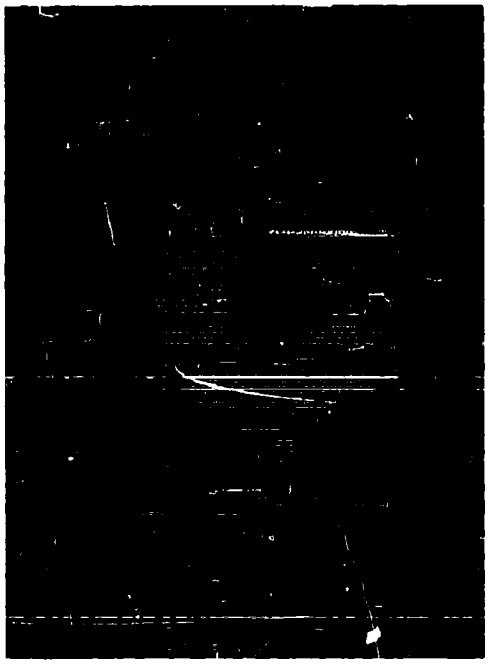


Fig. 4 - Oxide evaporation, intermediate results. Same procedure as in Fig. 3, except Ge was at room temperature. Photo shows an evaporated dot (center dot) surrounded by a region of no alloy (light area) & a region of alloy (small dark dots).

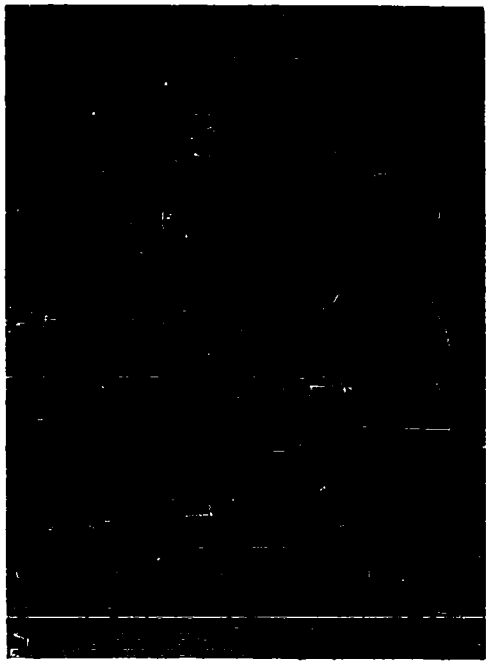


Fig. 5 - Oxide evaporation, best results. Shields 3 and 4 removed; shields 1 and 2, 1/8-inch holes; Ge at room temperature. A dot was evaporated and covered with gold. Photo shows an evaporated dot (center dot) surrounded by a region of no alloy (light area) and a region of alloy (small dark dots).

The noise figure F for a two-port network is defined as:

$$F = \frac{\text{Total Noise Power at Output}}{\text{Noise Power at Output Due to Source Resistance}}$$

This noise figure has been evaluated from transistor equivalent circuits by several authors. In particular, Guggenbuehl and Strutt (Ref. 3) computed a noise figure F, using the equivalent circuit of Fig. 6, which agreed with their experimental results.

$$F_{GS} = \frac{\alpha_{DC} \dfrac{\left|Z_s + r_e + r_b'\right|^2}{\left|\alpha\right|^2} - \left|Z_s + r_b'\right|^2}{4 r_e r_s}$$

where $\alpha_{DC} = I_c/I_e$, the ratio of dc collector current to dc emitter current.

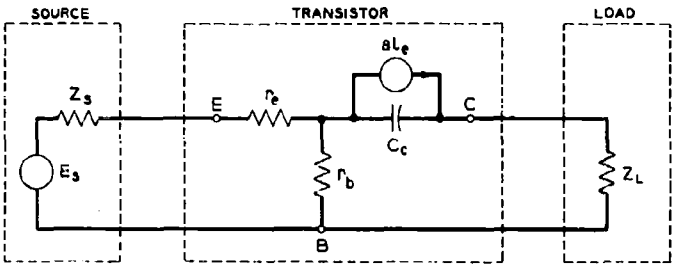


Fig. 6 - Equivalent circuit for noise figure calculation

Another noise figure computed by Nielsen (Ref. 4) using the same equivalent circuit is:

$$F_N = 1 + \frac{r_b'}{r_s} + \frac{r_c}{2r_s} + \frac{\left[(1 - a_o) + \left(\frac{f}{f_a}\right)^2\right]\left[r_s + r_b' + r_e\right]^2}{2a_o r_e r_s}$$

This noise figure separates the noise contribution of the transistor into three components: a component due to base resistance r_b', a component due to emitter current I_e, and a component due to the collector current that is not correlated with the emitter current.

If the source impedance is resistive, so that $Z_s = r_s$, then the relation between these two noise figures is

$$F_{GS} = \frac{\alpha_{DC}}{\alpha_o} F_N + \left(\frac{\alpha_{DC}}{\alpha_o} - 1\right)\left(\frac{(r_b' + r_s)^2}{2r_e r_s}\right)$$

For most transistors, $\frac{\alpha_{DC}}{\alpha_o} \approx 1$, so that $\left(\frac{\alpha_{DC}}{\alpha_o} - 1\right)\left(\frac{[r_b + r_s]^2}{2r_e r_s}\right)$ is small compared to F_N and $F_{GS} \approx F_N$, and Nielsen's noise figure agrees with Guggenbuehl and Strutt's. F_N was computed for the proposed transistor as a function of series base resistance r_b' at a frequency of 1 Gc, a source resistance of 50 ohms, and an emitter current of 1 ma. Figs. 7 and 8 show F_N as a function of r_b' for two values of α_o. For the proposed transistor, design values of f_a = 6 Gc, r_b' = 40 ohms, and α_o = 0.95 (see Ref. 2) seem reasonable. These values give a calculated noise figure of 4 db at 1 Gc.

1.4.1 Comments on Noise Figure

The noise figure shown in Figs. 7 and 8 are for a source resistance of 50 ohms and an emitter current of 1 ma. It is well known (Refs. 3, 4) that, for most transistors, the noise figure increases with increasing emitter current, so that a smaller emitter current should give a lower noise figure. However, since the input

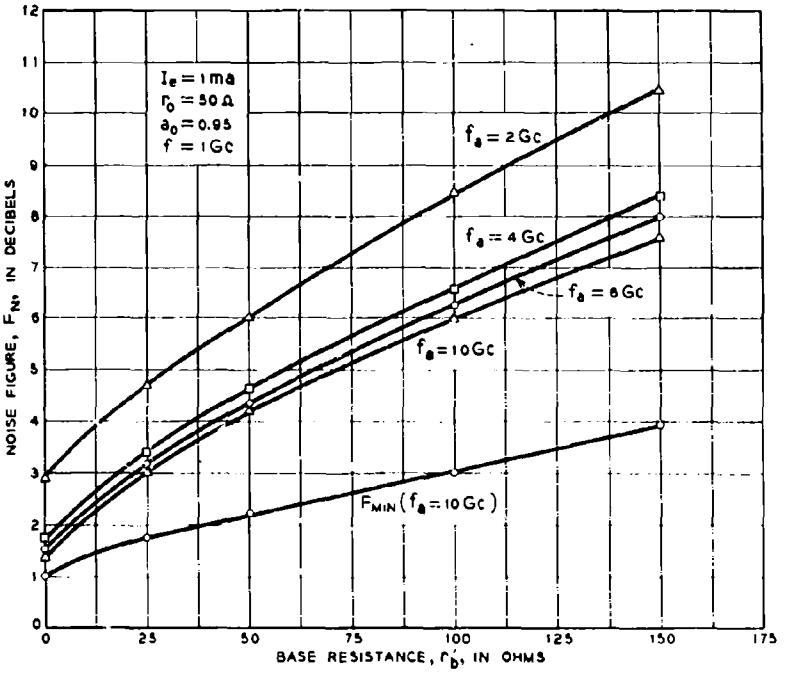


Fig. 7 - Noise figure, F_N, versus base resistance, r_b' with $a_0 = 0.95$

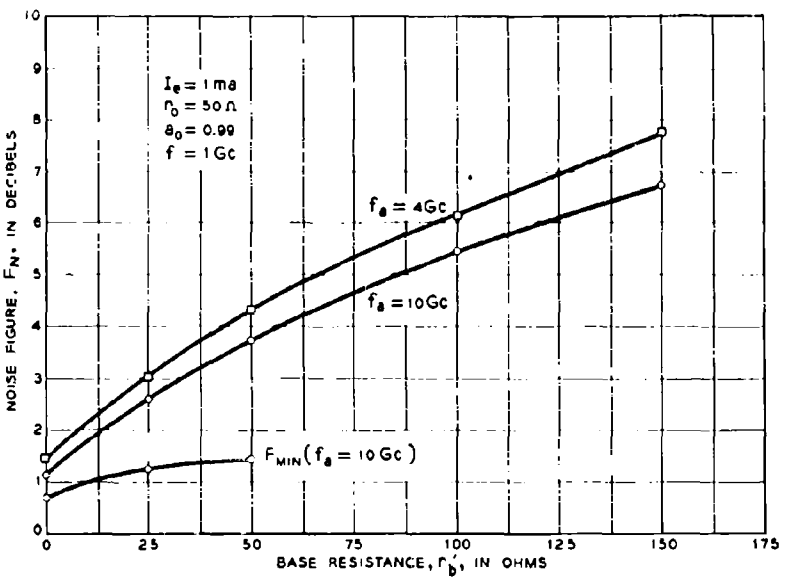


Fig. 8 - Noise figure, F_N, versus base resistance, r_b' with $a_0 = 0.99$

impedance of the transistor increases and α_0 decreases with decreasing emitter current, the gain decreases with emitter current. The value of 1 ma was chosen on the basis of experience with similar transistors, as a minimum current for which the transistor has reasonable gain. A lower noise figure can also be obtained by adjusting the value of source resistance until the noise figure is a minimum (Ref. 4).

The values of minimum noise figure and source resistance for minimum noise figure are shown in Figs. 7, 8 and 9. As shown in Fig. 9, the source resistances for minimum noise figure are greater than 50 ohms and are mismatched to the input impedance of the transistor (Ref. 2). The resulting amplifier would have lower gain and bandwidth than a matched amplifier, and the noise of the following stage might become important. For this reason, the source resistance of 50 ohms seems a reasonable compromise between gain and noise figure.

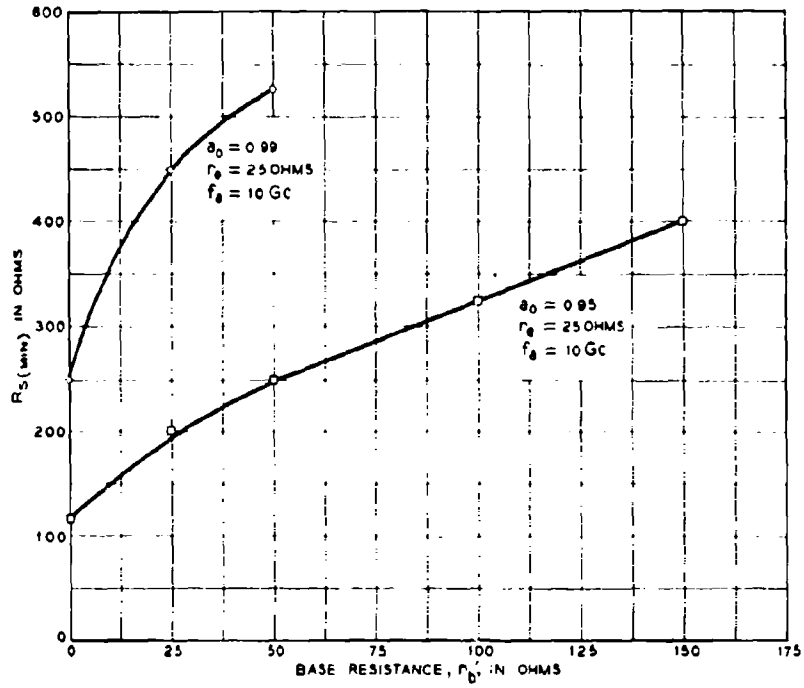


Fig. 9 - Source resistor for minimum noise figure versus base resistance

1.5 SUMMARY AND CONCLUSIONS

Techniques for evaporating oxides onto germanium have been studied in an attempt to control scatter from the oxide evaporation. The scatter has been reduced to give device quality results.

A calculation of noise figure for the proposed transistor shows that, with typical values of source impedance and emitter current, a noise figure of less than 5 db at 1 Gc should be possible.

REFERENCES

1. J. T. Nelson and R. E. Davis, "Status of the Microwave Transistor," Report No. 6 on Transistors, Contract DA 36-039 sc-88931, 31 December 1961.
2. A. G. Foyt, "The M2275, A Germanium Microwave Transistor with Circular Electrodes," Report No. 7 on Transistors, Contract DA 36-039 sc-88931, 31 March 1962.
3. W. Guggenbuehl and M. J. O. Strutt, "Theory and Experiments on Shot Noise in Semiconductor Junction Diodes and Transistors," Proc. IRE, 45, pp. 839-854, June 1957.
4. E. G. Nielsen, "Behavior of Noise Figure in Junction Transistors," Proc. IRE, 45, pp. 957-963, July 1957.

Chapter 2

STATUS OF THE M2260, A ONE WATT, ONE KMC TRANSISTOR

By R. E. Davis

2.1 INTRODUCTION AND SUMMARY

Work during this interval has been concentrated on the fabrication of the oxide-spaced structure. The modified evaporation jig has consistently produced evaporated structures within the tolerance limits allowed in the initial design, and results to date show the possibility of reducing the tolerance limits from ±1 mil to ±0.2 mil. This reduction of the tolerance limits would increase the stability and bandwidth of the unit by decreasing stray capacities. The scattering of SiO during evaporation has been decreased but not eliminated. Many of these units show emitter-to-base shorts, and it has not been determined whether this is caused by pinholes in the oxide, or by surface alloying under the oxide. Units without shorts have shown transistor action with a common-emitter current gain of 8.

Mesa units have been used for characterization during this interval since no completed oxide-spaced units have been available.

High frequency y-parameter measurements were taken for three 3-stripe mesa units with 1 x 20 mil stripes. All these units exhibited an abnormally high value of g_{22} at 1 kmc and above, giving a unilateral gain at 1 kmc of approximately 2 db. An explanation of this effect, consistent with the measurements, has been derived by considering the resistance in series with that part of the collector capacity which is not directly under one of the base electrodes. The calculation of this series resistance from measurements and calculated equivalent circuit element values, gives a value consistent with the mesa border and base doping.

The design for a new M2260 header is discussed, including preliminary electrical measurements, and the calculation of its thermal properties.

2.2 FABRICATION OF OXIDE-SPACED UNITS

The mesa evaporation jig used for the initial evaporations of the oxide-spaced structure required modification, as previously reported (Ref. 1). This modified jig has consistently produced an evaporated structure that is well within the tolerance limits allowed in the initial design of the structure. Experience to date indicates the feasibility of decreasing the tolerance limits. Table 2-1 gives the initial design dimensions for this structure, which allow ± 1 mil tolerance in the placement of the

Table 2-1

DIMENSIONS IN MILS OF THE OXIDE-SPACED STRUCTURE FOR ± 1 MIL TOLERANCE AND FOR ± 0.2 MIL TOLERANCE

Tolerance	W_e	W_b	ℓ	s	W_1	ℓ_4	ℓ_1	ℓ_2	ℓ_3	ℓ_5	W_2
± 1 mil	0.6	0.6	4.5	0.2	2	23	2	1	1	1	1.5
± 0.2 mil	0.6	0.6	4.5	0.2	2	23	0.7	0.2	0.8	0.2	0

evaporation pattern with respect to the diffusion masking hole in the SiO, and leaves a 1-mil wide emitter bonding strip on the SiO. The dimension parameters used in Table 2-1 are defined in Fig. 10. The inactive portions of the emitter and base electrodes give rise to parasitic capacities C'_{bc} and C'_{ec}. The capacity C'_{bc} from base to collector adds to the output capacity of the unit and decreases the bandwidth, and C'_{ec}, the feedthrough capacity from input to output, decreases the electrical stability of the unit. In the initial design given in Table 2-1, C'_{ec} = 1.3 pf and C'_{bc} = 1.8 pf at 10 volts collector bias. It is felt that the proposed dimensions shown in Table 2-1, which allow only a ± 0.2 mil tolerance, will provide a reproducible structure. In this

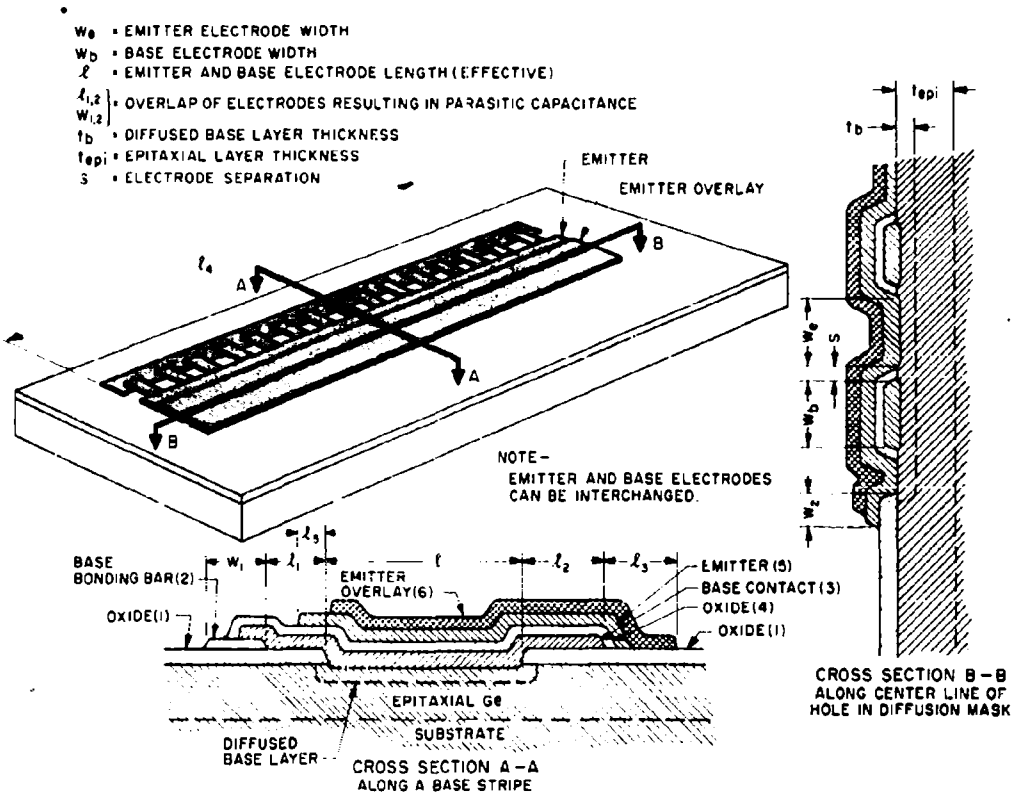


Fig. 10 - Interdigitated structure

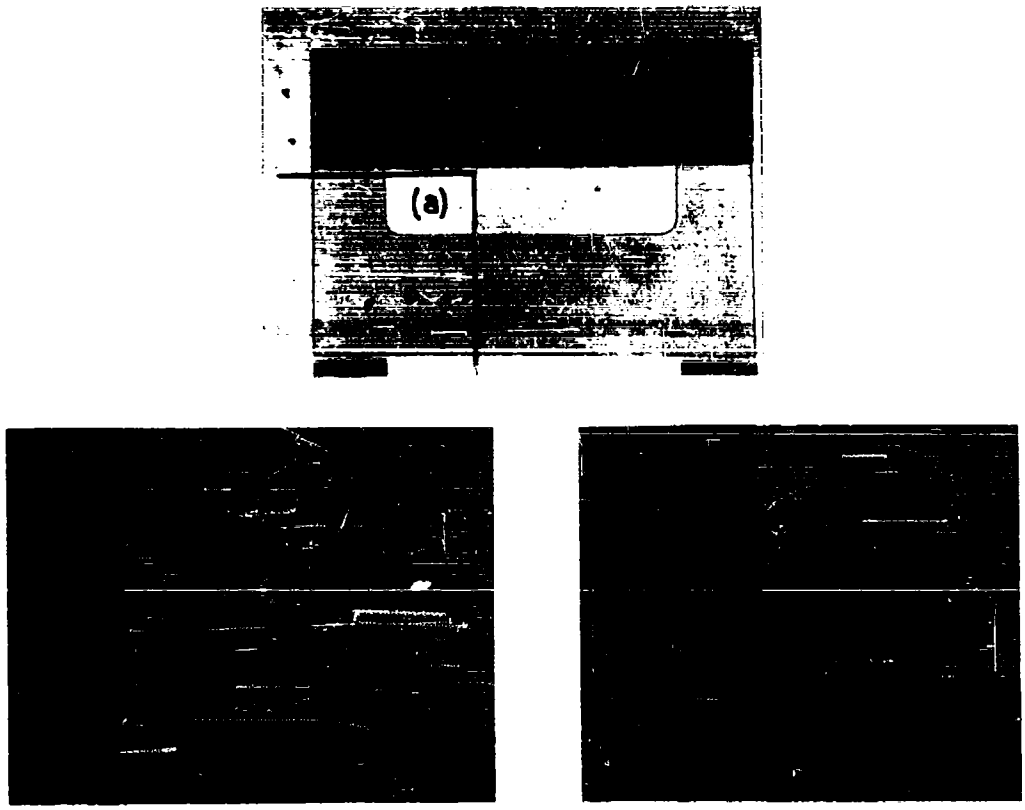


Fig. 11 - (a) Full diffusion mask showing section depicted in enlarged photos, (b) inside edge of diffusion mask before evaporation improvement and (c) inside edge of diffusion mask after evaporation improvement

case C'_{ec} = 0.37 pf and C'_{bc} = 1.1 pf. This reduces the feedthrough by a factor of 3, from that of the initial dimensions. If it is possible to bond the emitter leads directly over the active area of the transistor without deteriorating the junctions, the emitter bonding strip would not be necessary, and in this case C'_{cc} could be reduced to 0.066 pf.

Difficulty has been experienced with the scattering of the SiO during evaporation. This interferes with the alloying of the subsequently evaporated metal electrodes. Scattering of the SiO during the evaporation of the diffusion mask has been substantially decreased by modification of the shielding and by reduction of source size. Figs. 11(b) and 11(c) show the edge of the evaporated SiO diffusion mask before and after the evaporator improvements were made. The edge of the SiO mask shows a much sharper demarcation in the second case. Appreciable scattering is still encountered during the second oxide evaporation however, when the base stripes are covered with SiO. Although scattering has been reduced by the methods described in Chapter 1, no satisfactory method has been found for completely eliminating scattering at this stage. The slab must be removed from the jig to remove the scattered SiO between the stripes before the emitter evaporation is carried out. This requires

a second step of precision jigging, but will provide an expedient means of obtaining experimental units until the scattering problem is solved.

Many of these oxide-spaced units have exhibited emitter-to-base shorts, and it has not been determined whether these are caused by pinholes in the oxide or by surface alloying under the oxide. Those units not suffering from emitter-base shorts or oxide scattering have shown transistor action with a common-emitter current gain of approximately 8.

2.3 ELECTRICAL MEASUREMENTS AND EVALUATION

High frequency y-parameter measurements were taken for three 3-stripe mesa units with 1 x 20 mil stripes. Fig. 12 shows Re y_{22} and Im y_{22} as a function of frequency for one of these units at 50 ma emitter current and 5 volts collector bias. The measured collector capacity for this unit at 5 volts bias was 13 pf, giving C_o = 10 pf and C_i = 3 pf. This value of C_o in series with the collector and base lead inductances of 0.64×10^{-9} henries should give a series resonance at approximately 2 kmc. This series resonance may be clearly seen in the curve of Im y_{22} in Fig. 12. The resonant behavior of Re y_{22} at approximately the same frequency is more difficult to understand. Its effect, however, is to decrease the unilateral gain of the unit, given by:

$$U = \frac{|y_{21} - y_{12}|^2}{4(g_{11}\, g_{22} - g_{12} g_{21})} \quad .$$

Both the measured and calculated values give a unilateral gain of approximately 2.5 db for this unit.

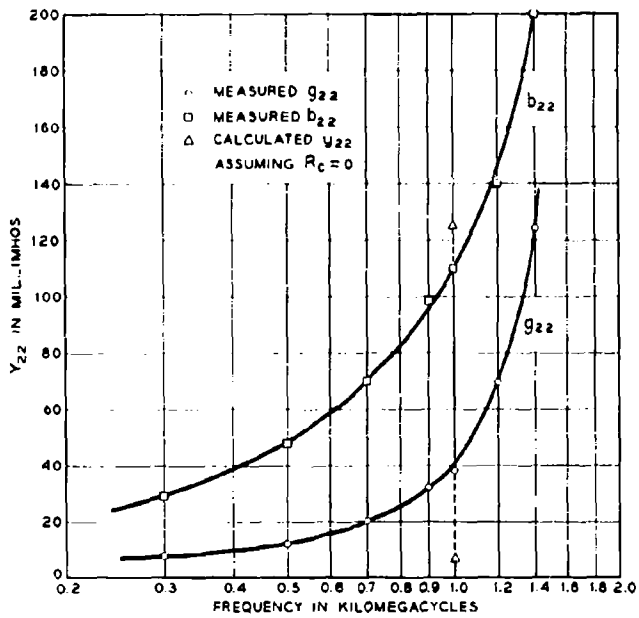


Fig. 12 - Y_{22} as a function of frequency for Unit No. 1

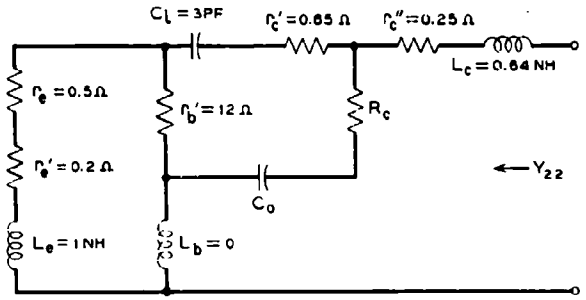


Fig. 13 - Equivalent circuit for the calculation of Y_{22}

A plausible explanation for this resonant behaviour of g_{22} will now be presented. In the mesa structure, the process of mesa masking leaves a border of diffused germanium surrounding the base electrodes. This additional outer capacity differs from that under the base stripes in that the charging current for this capacity must flow through the base sheet resistance. This effect may be accounted for by inserting an equivalent resistance in series with C_o in the equivalent circuit diagram. If this is done, and L_b ($\approx 4 \times 10^{-8}$ henries), and the αIe current generator are neglected for simplicity, the equivalent circuit diagram is as shown in Fig. 13. Using the measured value of y_{22} at 1 kmc from Fig. 12 and the element values shown in the diagram we may solve for C_o and R_c. When this is done we find C_o = 10 pf and R_c = 4.4 ohms. This value of R_c is consistent with the mesa fringe around the base stripes, and the base-doping level in this unit. A calculation based on this same circuit assuming C_o = 10 pf and R_c = 0 gives y_{22} = 7.32 + j125 millimhos. These values of g_{22} and b_{22} are plotted in Fig.12. Thus the insertion of 4.4 ohms resistance in series with C_o raises g_{22} from 7.32 to 41.5 millimhos, with an inherent decrease in unilateral gain.

The oxide-spaced structure, which does not have this extra border of diffused base surrounding the base electrodes should alleviate this problem. Other means of decreasing this effect are the use of heavier base doping, and a header with a lower value of L_c.

2.4 HEADER FOR THE M2260

A revised encapsulation has been designed for this transistor, in an effort to decrease the lead inductances as far as possible, as well as providing the necessary heat transfer. Fig. 14 shows the header design for the 1-watt, 1000-mc unit, for use in coaxial or strip-line circuits. The low inductance is obtained by making the encapsulation short and by using close-spaced diaphragms for the leads. The diaphragms will be connected to the transistor wafer by multiple short lengths of wire or by a foil.

In order that the stability and bandwidth of the wafer will not be seriously limited by the encapsulation, the emitter and base lead inductances should each be less than 0.05 nanohenries and the collector lead capacitance should be less than 1 pf (Ref. 2).

Although all the component parts are available, the brazing operation has not been developed to the point where the required tolerance can be met, so a prototype

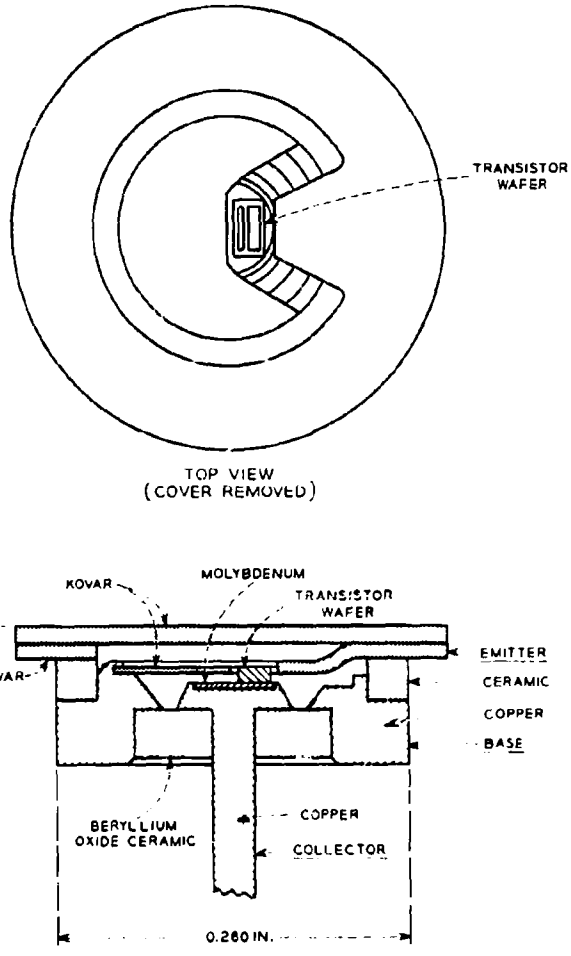


Fig. 14 - Encapsulation of 1-watt, 1000-mc transistor

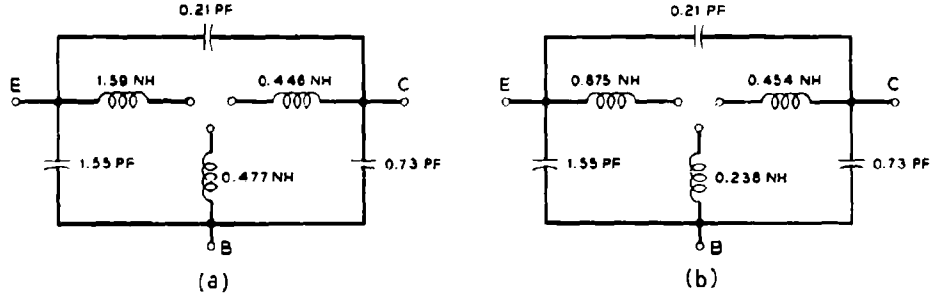


Fig. 15 - Equivalent circuit for the new header: (a) with four straight leads bonded to each electrode and (b) with four leads bonded to each electrode and the base leads spread out

header was cemented together for initial electrical testing. The stray capacity measurements shown in Fig. 15(a) prove to be satisfactory.

Four 0.4-mil diameter gold leads were bonded from the collector pin to the emitter tab, and four were bonded from the collector pin to the base diaphragm. The equivalent T derived from measurements on the 1607-A transadmittance bridge is shown in Fig. 15(a). The bonded leads from collector pin to the base diaphragm were then fanned out as far as possible on the base diaphragm to reduce the mutual inductance of the leads. The equivalent T derived from impedance measurements is shown in Fig. 15(b).

In this preliminary assembly, the emitter tab and base diaphragm were located too far above the collector pin and required bonding leads 25 mils in length. These long leads are at least in part responsible for the relatively high inductances observed, and the lead length must be shortened to approximately 10 mils in the final header.

The heat transfer in this header is obtained by the use of a beryllium oxide insulator between the copper collector lead and copper outer jacket. A molybdenum insert is required between the wafer and copper pin to match the semiconductor expansion coefficient.

2.5 THERMAL RESISTANCE OF THE M2260 TRANSISTOR

Exact analytical solutions for the thermal resistance of the M2260 wafer-coaxial header combination are indeed very complex. The simpler and almost as useful approach is to consider the wafer and coaxial header as two separate temperature distribution problems. This separation is accomplished by assuming that an isothermal surface exists between the bottom of the wafer and the top of the collector pin. This is an approximation, but from the analysis of the heat flow in the wafer it does not seem to lead to any gross errors.

Further, rather than seeking analytical expressions or machine solutions for these two temperature distributions, analogue techniques were developed to solve the two problems. The desirability of this method becomes apparent when the solution for temperature distribution in the coaxial header is considered. Even with cylindrical symmetry, the number of different conducting media and the complicated geometry of the header present a formidable system of boundary value problems to be solved. An electrical analogue is immediately suggested as the method of solution because of the correspondence of current, voltage, and electrical resistance to heat flow, temperature, and thermal resistance respectively. Physically the analogue is a water-bath model representing a two-dimensional differential cross section of either the wafer or the coaxial header. The different thermal conductivities are represented by varying the depth of the water.

Because of the rectangular geometry and single conducting medium of the wafer, the analogue technique for it is simply to determine the two-dimensional spreading factors from electrical resistance measurements on the water-bath model of the wafer. These spreading factors are then used to correct a simple parallel-plate thermal-resistance calculation. If the heat sources in the wafer are taken to be the twelve 0.0045 x 0.0006 inch emitter stripes, and the heat sink is a 0.010 x 0.020 inch isotherm at the bottom of the 0.004 inch thick wafer, then the thermal resistance of the wafer turns out to be 23°C/watt.

For the coaxial header, however, the water-bath model is not so easily applied because it represents a rectangular solid-shaped differential cross section. What is needed is a wedge-shaped differential section so that integration around the circle can be performed. Rather than incur the mechanical problems associated with building a wedge-shaped model, a mathematical correction is used which transforms the rectangular bath into a wedge-shaped bath.

The mathematical correction needed is to double all vertical (along the cylindrical axis) voltage differentials in the rectangular model's potential distribution and then multiply all radial voltage differentials, in the rectangular model, by R_0/r; where R_0 is the outside radius (the heat sink) of the header and r is the radius where the voltage differential occurs. Then these corrected voltage differentials may be added up along any convenient path of integration, extending from R_0 to the heat source at the center, to yield a new center potential (potential at the heat source). From the constant-current derivation of the transformation the ratio of resistances of the rectangular model to the wedge-shaped model is exactly the ratio of their respective center potentials. Thus the resistance of the wedge-shaped bath can be found, and after integrating this around the circle, a simple ratio of electrical to thermal conductivities yields the thermal resistance of the header. For this first calculation the collector pin has been assumed to be made entirely of molybdenum. Then, with a 0.020 inch diameter heat source at the top of the collector pin and a heat sink which is the entire outer circumference of the header, the thermal resistance of the coaxial header is 9°C/watt. (Assuming a BeO conductivity of 0.5 cal cm/sec/deg).

A simple addition of the two component thermal resistances, allowed by the assumption of the isothermal surface between the wafer and the collector pin, yields a thermal resistance of 32°C/watt for the entire transistor.

This value of thermal resistance is only just marginally acceptable, and some effort will be directed toward lowering this figure. From knowledge of the temperature distribution in the transistor it has been observed that most of the thermal drop takes place in the wafer and its immediate vicinity; therefore attempts will be made to decrease the wafer thickness and to use the proposed combination copper-molybdenum collector pin. In all of this work the analogue technique developed for calculating thermal resistances will be used extensively to predict the merits of any changes in wafer or header design.

REFERENCES

1. R. E. Davis, "Status of the M2260, 1-Watt, 1000-mc Transistor," Report No. 7 on Transistors, Contract DA 36-039 sc-88931, 31 March 1962.

2. M. J. Birck, "A Digital Computer Simulation and Stability Analysis of an Equivalent Circuit for the M2260 Power Transistor," Report No. 6 on Transistors, Contract DA 36-039 sc-88931, 31 December 1961.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Chapter 3

INTEGRATED CIRCUIT PACKAGE CLASSES FOR LAYOUT OPTIMIZATION

By B. T. Howard and R. Lindner

3.1 INTRODUCTION

In an earlier report (Ref. 1) the optimization of integrated package design for the most efficient layout of subsystem functions was considered. This chapter will extend the study by illustrating some of the criteria that will be used in approaching the problems of integrating other subsystem functions.

In particular, a number of subsystem functions have been studied to determine whether a flexible approach to integrated package design is, or is not, necessary to optimize the layout problem. Various classes of encapsulations will be discussed and then the optimum arrangement of devices to be integrated within the package will be considered with respect to the criteria of size of the layout, number of package types, number of packages and number of leads. Finally, the effect of these studies on integrated circuit technology will be discussed.

3.2 PACKAGE CONSTRUCTION

To obtain the optimum equipment layout several aspects of the package to be used must be considered. These include the size and shape of the package and the number and position of the leads as well as the number and type of devices to be integrated. There are also system considerations which affect the package design, such as the type of circuit board to be used and the degree of standardization which is desirable.

The optimum circumstances are difficult to define completely or exactly but for the purposes of this study the optima will be defined as those conditions which minimize the number of packages, the numbers of leads (or external connections) and the area of the circuit layout. With these criteria it is possible that a different package construction would be best for each grouping of devices. For example, the group of four grounded-emitter transistors, Fig. 16(a), would perhaps be best packaged with the four output (collector) leads on one side and the four inputs (base) leads on the opposite side. However, the multiple diode of Fig. 16(b) might well use

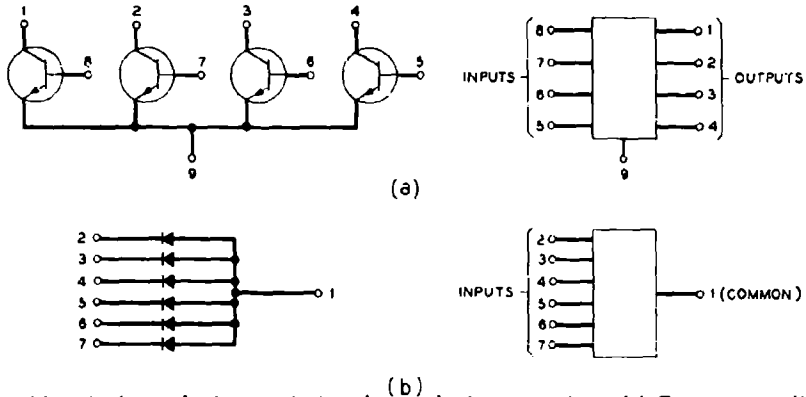


Fig. 16 - Package design variation due to device grouping. (a) Common-emitter transistor lead configuration. (b) Multiple-diode lead configuration.

a package with its six input leads on one side and the common lead on the opposite side.

A rectangular shape was used for these two illustrations, but a very common package is the circular type, typified by the T05.

The T05 header assembly has the present advantage of using established manufacturing techniques and is thus readily available. Therefore, the layouts for several subsystems are being developed using this package. The number of the available leads, of course, must be considered in the initial allocation of devices to packages.

3.3 TYPE OF CIRCUIT BOARD

To reduce the number of degrees of freedom in the study to a reasonable number, a single type of circuit board was considered. This was a standard type of single-sided printed-circuit board which has been used in a number of systems. The dimensions and spacing of the printed wires and solder lands on the boards to be discussed are those used in common practice. The wire stripes are 50 mils wide and the solder lands are a minimum of 100 mils in diameter. Also no spacing of less than 50 mils is allowed between conductor strips. The terminal tabs are also of a size that fit available connectors. These are 80 mils wide by 400 mils long on 114 mil centers.

The jumber wires are of 20 mil, tinned copper which is reasonably inflexible when mounted flat on the back side of the board. The resistors used are all 1/4 watt Allen Bradley resistors, the main body of which is 1/4 inch long by 3/32 inch diameter.

3.4 LAYOUT OF SUBSYSTEM FUNCTIONS

There are obviously many ways in which devices may be grouped within a single integrated package. Functional groups could be chosen such as binary

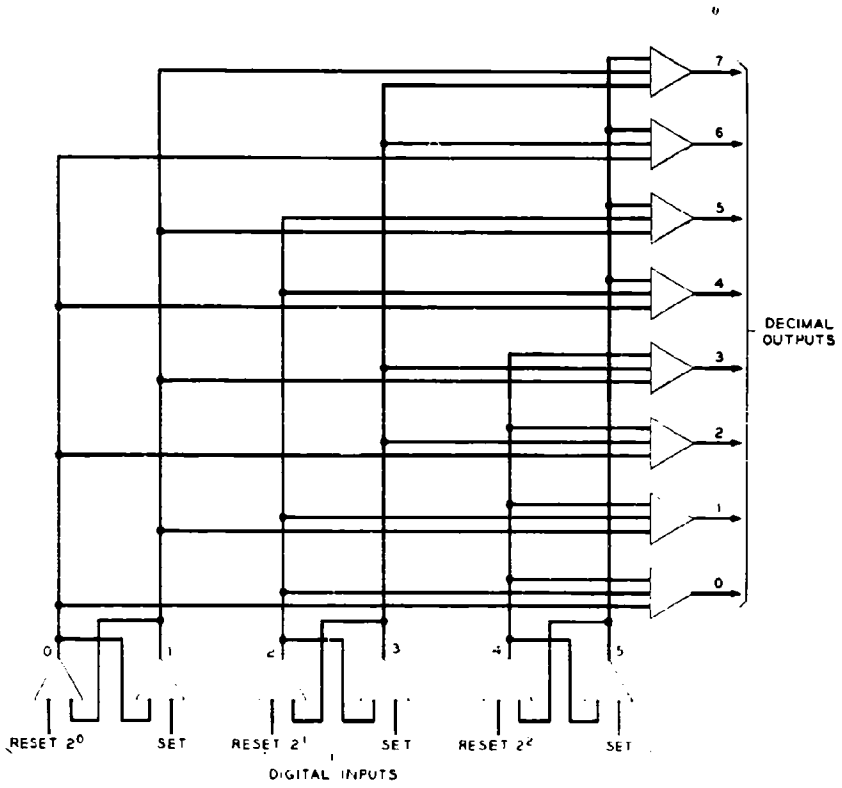


Fig. 17 - Schematic circuit of binary to decimal translator. Triangles represent low-level logic "and not" gates.

counters or low-level logic gates (Ref. 2). These functional groups are often repeated many times in a system and hence a reasonably restricted number of package codes could be selected for a system. On the other hand, multiple-like devices such as multiple diodes (Ref. 3) or common-emitter transistors could be used in system design with an equal degree of standardization of package codes. The choice between these two approaches is not obvious, nor easy to generalize. To elucidate the problem, three examples will be considered and a comparison made of the two approaches with respect to their effect on the equipment layout for the subsystem functions.

1. Binary-to-Decimal Translator: The first example to be considered is a binary-to-decimal translator which is shown in Fig. 17. This is an example of a highly iterative circuit using the low-level logic gate as a basic element. Six low-level logic gates interconnected as three flip-flops receive the binary input pulses. These flip-flops are connected to eight gates from which are obtained the decimal outputs.

An obvious functional group to be considered is a package containing a single gate. The layout for the translator using this package is shown in Fig. 18 and the relevant statistics are listed in Table 3-1.

The alternate approach of using multiple-like devices requires three package types (multiple input diodes, multiple level-shifter diodes and multiple transistors).

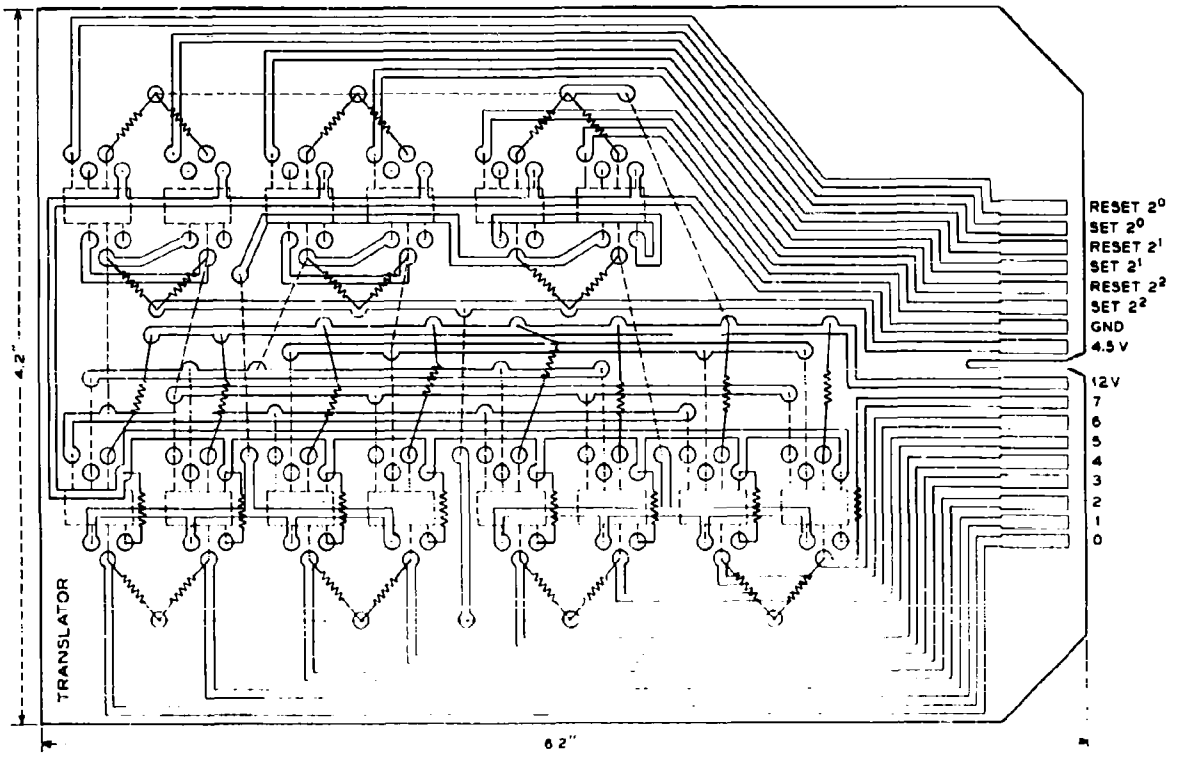


Fig. 18 - Layout plan of translator on printed-wire board using functional packages containing a single "and not" gate. Dashed lines are jumper wires.

TABLE 3-1

Class of Package	Functional	Multiple
Number of Package Types	1	3
Total Number of Packages	14	6
Total Number of Leads	98	98
Area of Layout	25.6 sq. in.	20.5 sq. in.

The layout that results from the use of these packages is shown in Fig. 19 and the relevant statistics compared with the functional approach in Table 3-1.

It can be seen that the multiple-device layout is considerably more efficient than that resulting from functional packages. Not only is the layout simpler but its size is considerably reduced.

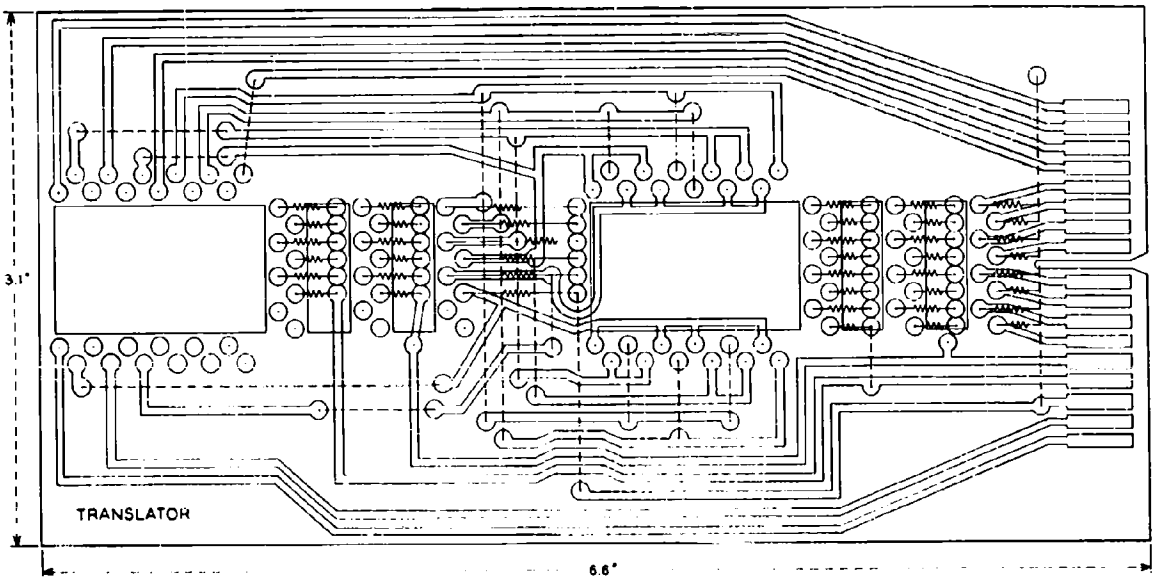


Fig. 19 - Layout plan of translator on printed-wire board using multiple device packages. Package A contains eight common-emitter transistors, package B contains eight level-shifter diodes, and package C contains 24 computer-diodes.

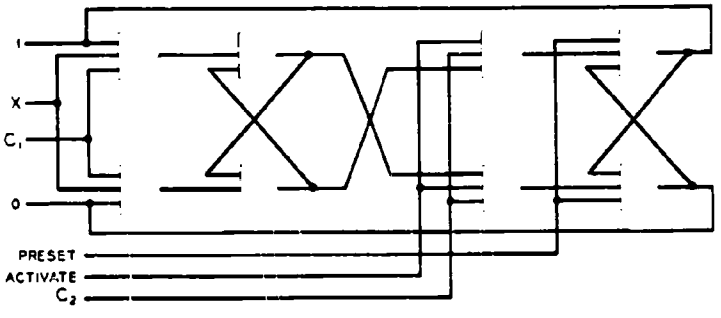


Fig. 20 - Schematic circuit of a stage of a binary adder designed for non-racing. Triangles represent low-level logic "and not" gates.

2. Binary Adder: Another subsystem which also employs the low-level logic is a stage of a binary adder designed for nonracing. The adder, shown in Fig. 20, consists of eight gates. The result of a functional layout and a multiple-device layout are shown in Figs. 21 and 22, respectively. The same packages as before were used in developing these arrangements. The relevant statistics for the two arrangements are shown in Table 3-2. The results show that the large advantage of the multiple case, obtained with the translator, no longer exists and the two approaches are directly comparable. The difference in the subsystems is that the translator requires outputs from eight gates to appear at the terminals and thus

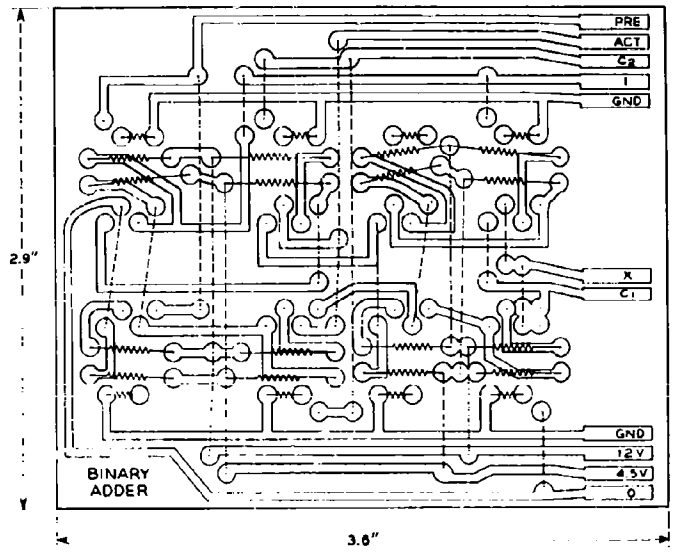


Fig. 21 - Layout plan of binary adder on printed-wire board using functional packages containing a single "and not" gate.

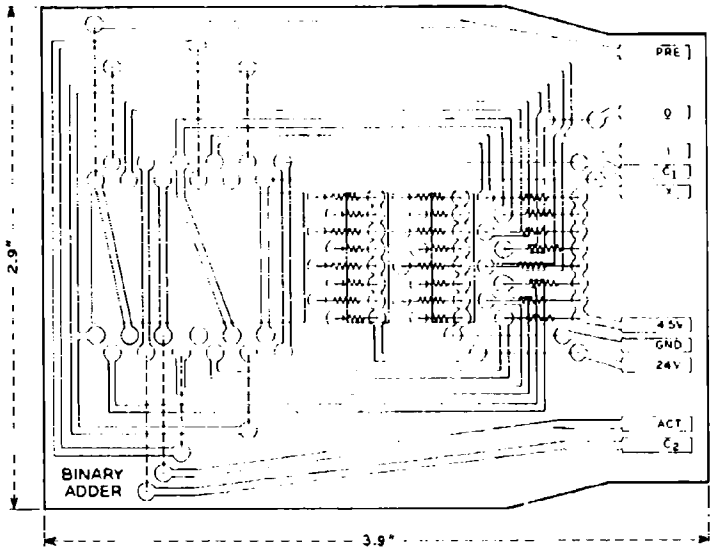


Fig. 22 - Layout plan of binary adder on printed-wire board using multiple device packages.

having these eight outputs appear side by side from a single package is highly efficient. The binary adder, however, has only two outputs of gates appearing at the terminals and the coupling of gate outputs in a single package is not as important.

TABLE 3-2

Class of Package	Functional	Multiple
Number of Package Types	1	3
Total Number of Packages	8	3
Total Number of Leads	56	55
Area of Layout	10.4 sq. in.	11.3 sq. in.

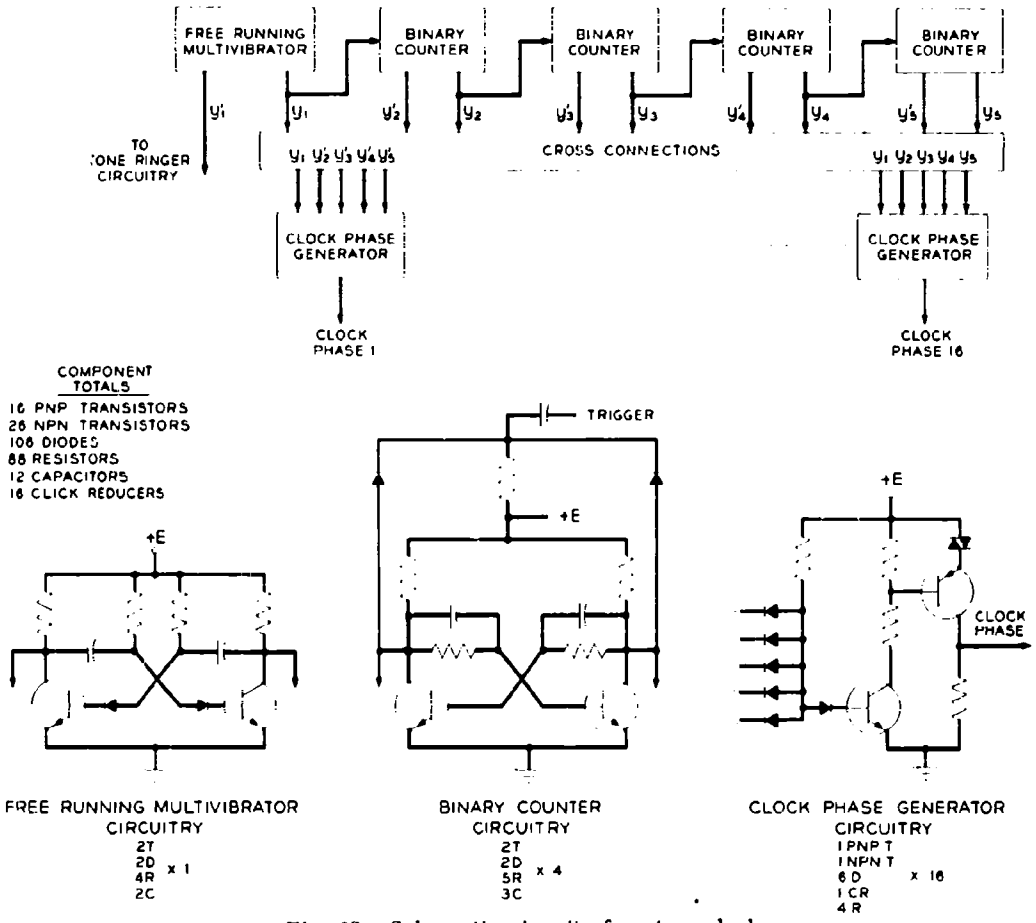


Fig. 23 - Schematic circuit of system clock.

3. System Clock: A third example of a system subfunction is the system clock shown in Fig. 23. Here again, a decision whether to make multiple-device packages or functional packages is to be made. In this case an additional constraint will be imposed in that the T05 header assembly is to be used. This assembly can have

TABLE 3-3

Multiple Device Design	Number of Devices	Number of Packages	
		8 Lead Header	9 Lead Header
Transistor (Com. Emit)	26	9	7
PNP Transistor	16	8	6
Click Reducer	16	3	2
Double Diode	4	2	2
Single Diode	2	1	1
Sextet Diode	16	16	16
		39	34

TABLE 3-4

Functional Design	Number of Devices	Number of Packages	
		8 Lead Header	9 Lead Header
Multivibrator	1	1	1
Binary Counter	4	4	4
Phase Generator			
a. Sextet Diode and Transistor	16	16	16
b. PNP + Click Red.	16	16 (6)	16 (4)
		37 (27)	37 (25)

eight or nine leads and the number of packages required in each case will be determined. Table 3-3 shows the package breakdown for a strictly multiple device design. The first column indicates the number of each device needed; the second column, the number of packages needed for this device for an eight lead header; and the third column, for a nine lead header. Summing the columns shows 39 packages are needed with 8 leads and 34 packages are needed with 9 leads. Combining the single and double diodes would reduce these sums by one.

If a strictly functional design is used, i.e., where the multivibrator, binary counter, and clock phase-generator circuits are to be integrated as blocks, then the packages required are shown in Table 3-4. Here 37 packages are needed for either eight or nine lead packages. However, if a concession is made to allow several emitter-follower transistors with their associated click reducers to be put into a single package, then the number of packages needed (number in parenthesis) is 27 with eight leads and 25 with 9 leads. The 27 should be compared to 39, and 25 compared to 34. Thus for the clock circuit, the functional approach with slight hybridization requires many less packages than the multiple-device approach. It can also be shown that the layout space of the total circuit required for the functional packages is much less.

3.5 CONCLUSIONS

The problem of determining the correct configuration and device grouping of integrated packages does not possess a unique solution. As shown by the three subsystems considered, the multiple-device approach to packages as opposed to the functional-device approach can be greatly superior, nearly alike, or greatly inferior. The packaging techniques should be flexible enough to enable the procedure to be used which best fits the needs of the particular subsystem to be integrated. The construction of the package must also, if possible, be flexible in the number and positioning of leads so as to make for an orderly flow of the circuit as it is laid out on the printed-circuit board.

It may be found that standardizing on a group of package types will be possible after looking at a large number of systems. These packages might also prove useful in the design of new systems. But at this point, a degree of freedom in allowing new package types to be designated with a particular circuit in mind is required to best realize the promises of integration.

REFERENCES

1. R. Lindner, D. A. Naymik, Report No. 6 on Transistors, Contract DA 36-039 sc-88931, 31 December 1961, Chapter 5.
2. M. M. Atalla, Report No. 5 on Transistors, Contract DA 36-039 sc-88962, 3 August 1961, Chapter 3.
3. E. G. Walsh, Second Interim Technical Report on Transistors, Contract DA 36-039 sc-85352, 30 November 1960, Chapter 10.

Chapter 4

THE INFLUENCE OF EVOLVING TECHNOLOGY ON INTEGRATED CIRCUITS

By B. T. Howard and R. Lindner

4.1 INTRODUCTION

In the previous chapter an examination was made of the effect of different device groupings in an integrated circuit package on the layout of various subsystem functions. One of the conclusions drawn was the need for flexibility to be maintained if an optimum solution was required. There is another aspect in which flexibility must also be maintained, that of the ability of the integrated circuit technique to absorb easily the advantages offered by the evolution of the component and equipment technologies. In other words, the integrated circuit technology should, ideally, be able to take advantage of any progress in any related technology without a prolonged period of difficult retooling or redesign.

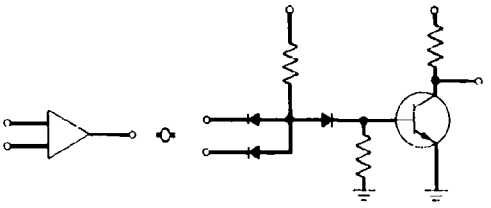
This chapter will report the results of a study made to determine the effects of changing technology on the integration of a particular subsystem function. In particular, four variations on the integration of a 24-bit register have been studied with respect to package design, circuit layout and the relevant statistics. In this case the relevant statistics are considered to be the number of package types, the total number of packages, the number of leads (or external connections), the layout area and the equipment volume needed for the complete 24-bit register.

4.2 THE 24-BIT REGISTER

The 24-bit register which was used for this study is shown in Fig. 24. Each bit is made up of five low-level logic gates (Ref. 1) which comprise input gates, a flip-flop (used as the storage element) and an output gate. The particular register is constructed with 24 identical circuits of this type using a total of 120 gates.

4.3 INTEGRATION TECHNIQUES

1. Semiconductor Integration — T05 Package: The first study was made with the assumption that a 9-pin T05 package would be used and that only semiconductor devices would be integrated within the package. It was further assumed that the packages would be assembled on a conventional single-sided printed-circuit board. The resulting layout for 4 bits of the register is shown in Fig. 25 and contains 15 packages made up of two different codes. The devices in the two package



LOW-LEVEL LOGIC GATE SYMBOL

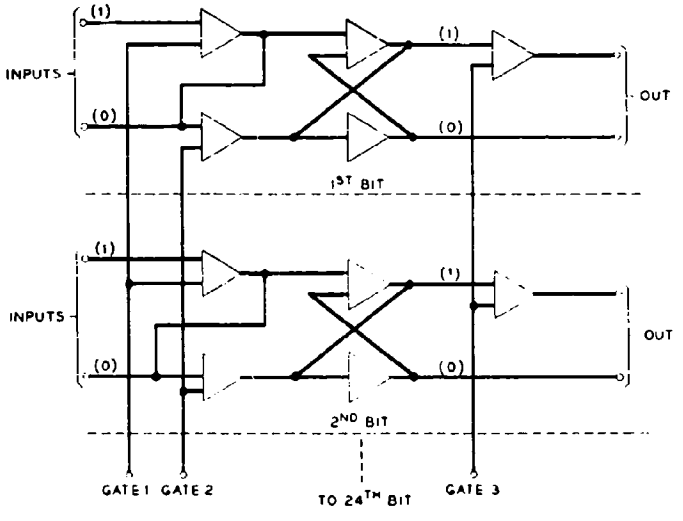


Fig. 24 - Schematic of 24-bit register. Triangles represent low-level logic gate as shown in upper part of figure.

types are shown in Fig. 26. The inverter-amplifier transistors from four gates are encapsulated in one package type while the level-shifter diode and input diodes from two gates are encapsulated in the other. Thus, three packages are necessary for four low-level logic gates. In accordance with the boundary condition, the resistors necessary for the completion of the gates are incorporated separately as individual components.

2. Semiconductor Integration – Ceramic Package: The only changes made in the assumptions for this case were that a multileaded ceramic package of rectangular form would be used and that only multiple-like devices would be used. Three types of integrated packages, all of the multiple-device type are necessary. One contains the input diodes for four gates, the second contains the same number of level-shifter diodes; the third contains the transistors necessary to complete the gate. The layout, shown in Fig. 27, does not differ greatly from that of the first case. This is primarily because the limitations of the circuit board dominate in both cases. Thus, no great advantage will accrue from the development of sophisticated package designs unless the circuit board is also designed to take advantage of the package development. This statement may be phrased, positively, by saying that

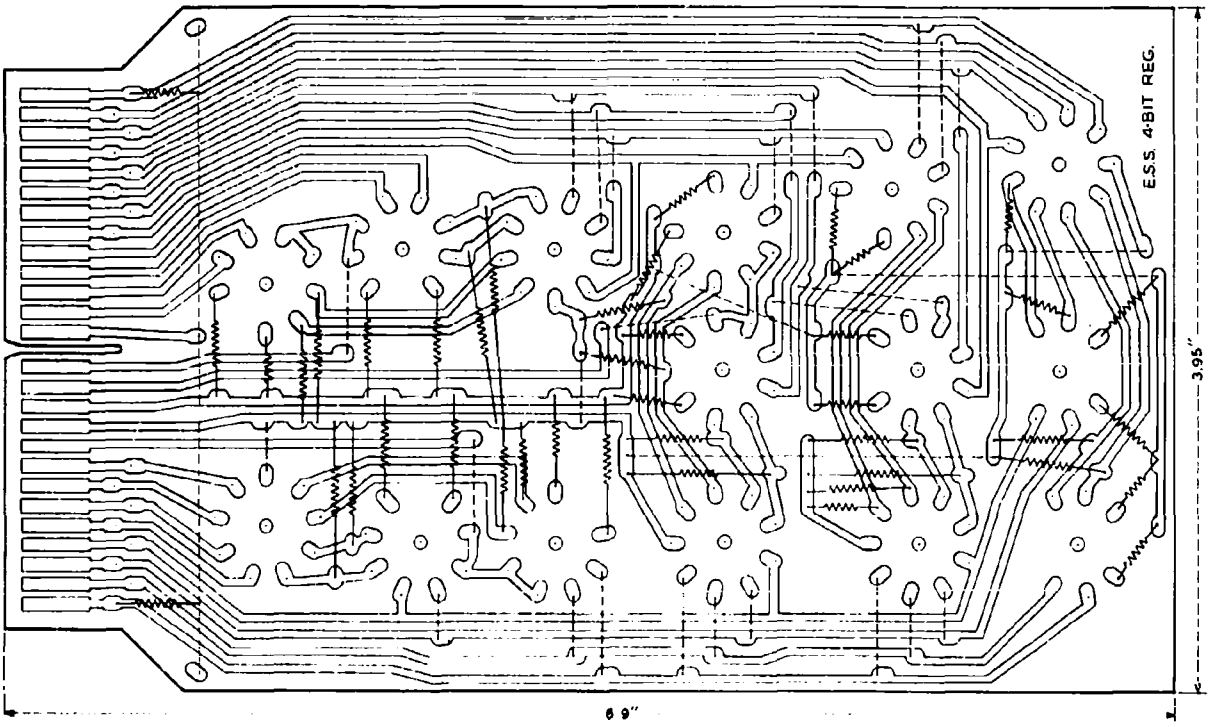


Fig. 25 - Layout plan of 4-bit register on printed-wire board using T05 header assemblies and external resistors.

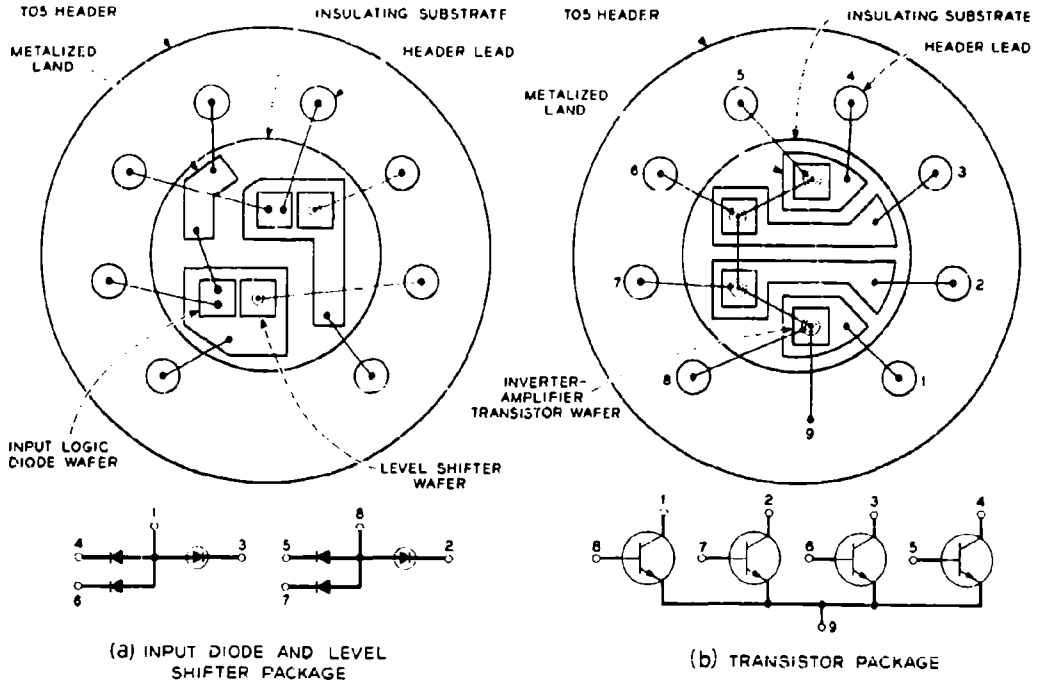


Fig. 26 - Package design for layout with external resistors. (a) Input diode and level-shifter package. (b) Transistor package.

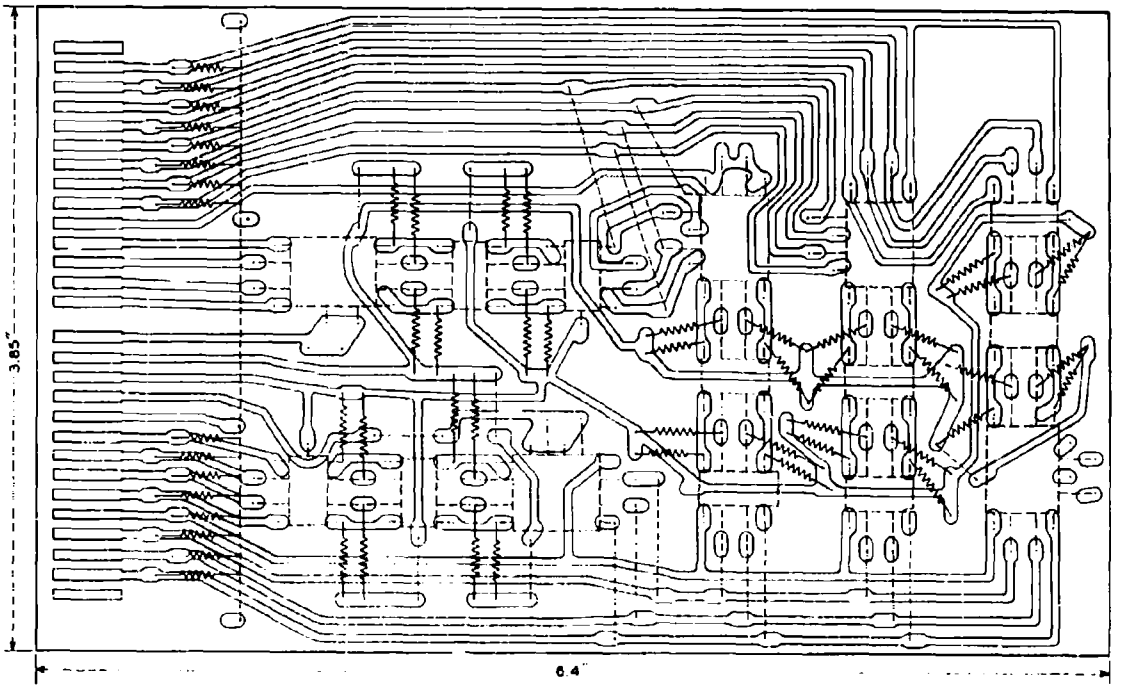


Fig. 27 - Layout plan of 4 bit register on printed-wire board using ceramic packages.

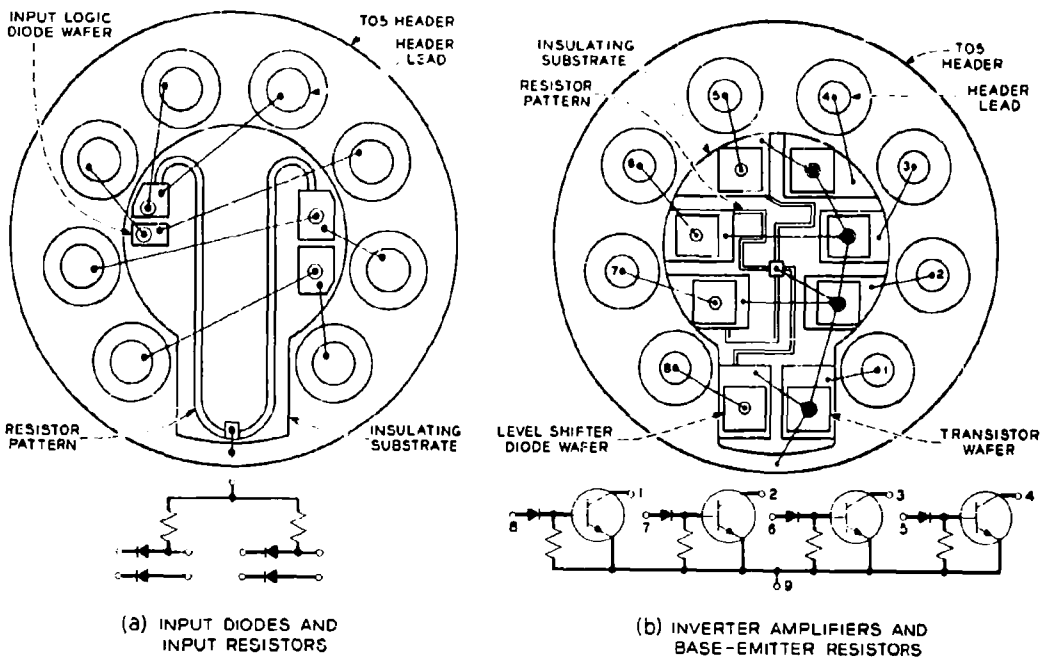


Fig. 28 - Package design for layout with resistors in packages. (a) Input diode and input resistors. (b) Inverter amplifiers and base-emitter resistors.

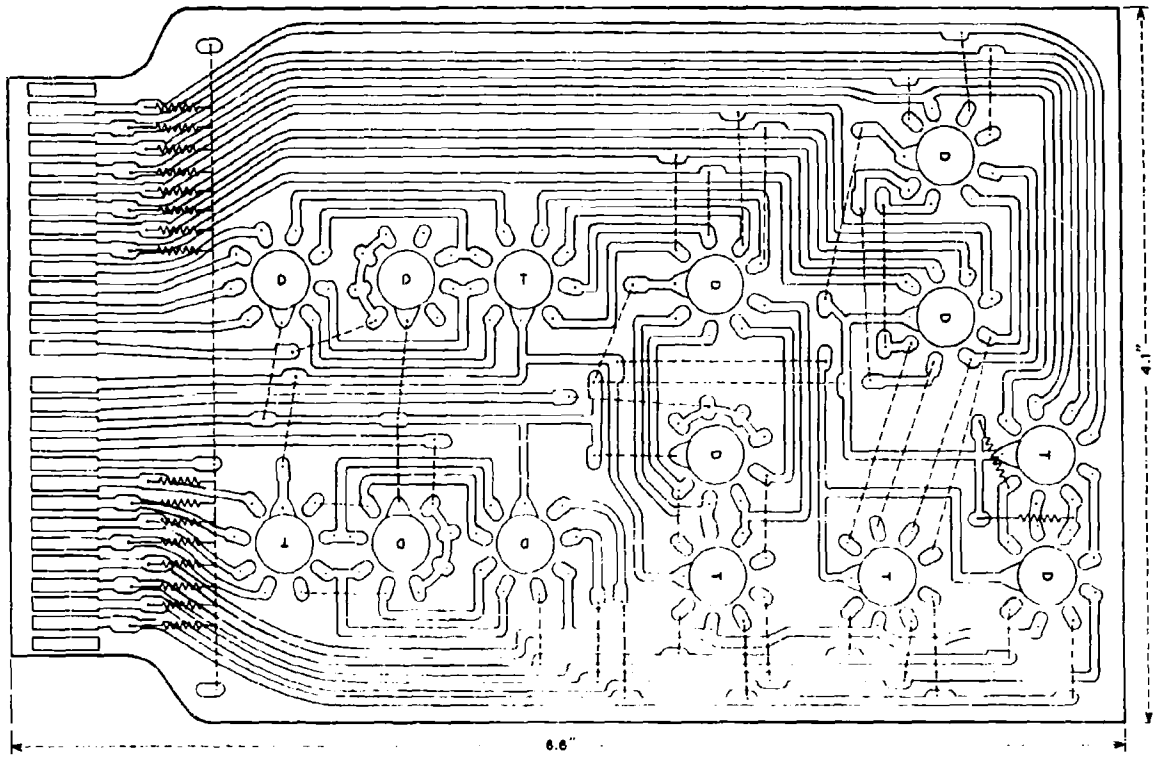


Fig. 29 - Layout plan of 4-bit register on printed-wire board using T05 header assemblies with internal resistors.

the use of multileaded T05 packages enables substantial gains to be made when they are combined with standard circuit boards.

3. Semiconductor-Resistor Integration – T05 Package: The next stage to be considered is the integration of both semiconductor devices and passive components (in this case, resistors only) in the same multileaded T05 package. Here, the assumption is made that the two types of components are mutually compatible as far as any necessary common processing is concerned. Further, the two types of components are required to fit within the same area. To determine what film resistors could be incorporated, assumptions had to be made as to the possible values of sheet resistivity, line width and line separations. The values assumed are those which have already been achieved by the tantalum resistor technology (Ref. 2). As a result, it was found to be possible to incorporate two of the three gate resistors in the packages, but the third, the load resistor, was treated as a separate standard component.

In this case two types of packages were used, as shown in Fig. 28. The first contains the input diodes and supply resistors for two low-level gates. The second contains the corresponding level-shifter diodes, transistors and emitter-base resistors. In the resulting layout of the 4-bit register on the board, Fig. 29, fourteen packages were necessary. The size of this layout again does not differ significantly from the first but, as will be discussed later, a considerable simplification in the interconnection problem is obtained through the component grouping which is used.

4. Semiconductor-Resistor Integration — Double Plane Ceramic Package: In this the final case, several important restrictions were removed. It was no longer assumed that the package must be assembled on a standard circuit board but a three-dimensional arrangement was used. It was also assumed that two planes could be used in each package, one for active components, and the other for passive components.

Because these new boundary conditions are further removed from standard practice, the package and equipment design will be discussed in some detail. However, it should be realized that the details are only used for illustrative purposes and that they do not necessarily represent the most practical or the best solutions to the particular design problems. Nevertheless, the range of speculation has been restricted and only solutions which required development as opposed to invention were allowed.

The first question to be considered is the amount of circuitry to be placed in the ceramic package. It was found that considerable simplification could be obtained if four complete low-level logic gates (resistors as well as active elements) were put in a single package. The register requires five gates to obtain a single bit. Therefore, if five packages are used, four bits can be constructed. Repeating this six times provides the entire 24-bit register.

The shape, size, and terminal locations of the package must be decided, consistent with the best three-dimensional arrangement and the layout of elements in the package. The method used here was to base the shape and terminal location entirely on providing an optimum arrangement; and use only the size as the variable to allow the internal element layout. The package shape that seemed to be best was a thin rectangular box with the eight input terminals on one end and with the four output and three voltage terminals on the opposite end. This is shown in Fig. 30.

The optimum three-dimensional arrangement of these packages which can be called "gate" packages into a composite package called a "4-bit" package is shown in Fig. 31. The five gate packages are stacked in a particular way and plugged into an "L" shaped piece having the appropriate printed circuitry. A terminal piece providing additional interconnections is attached and finally a container is slipped over and crimped to enclose the package. The 4-bit package, exclusive of terminals, is approximately 0.4" x 0.6" x 0.7". There are 83 connections made involving the frame and the gate packages. The terminal area contains 22 terminals.

It should be noted that the interconnection pattern of printed circuitry is surprisingly simple considering the length of wiring needed in two-dimensional board design of the circuit. An idea of the volume savings that has been obtained can be seen by comparing it with the present printed-board circuitry. Here 15 boards require 140 cu. in. to provide a 24-bit register. The three dimensional design (six 4-bit packages) requires 1 cu. in. This small volume may have a heat problem, but considerable features could be added to alleviate that problem and still obtain a sizable space reduction.

Now, we must retrace our steps back to the construction details of the gate package. For if the "finished product" of Fig. 31 looks promising, then it is important that the technologies that might be used in its construction be recognized.

It was decided to put four low-level logic gates in the gate package. This means that these items are required: four transistors, four level-shifter diodes, four double-computer diodes, four 10,000 ohm, four 560 ohm, and four 4700 ohm resistors. It was assumed that metal-film resistors would be used. These have the advantage of good control of high values, good temperature stability and small size.

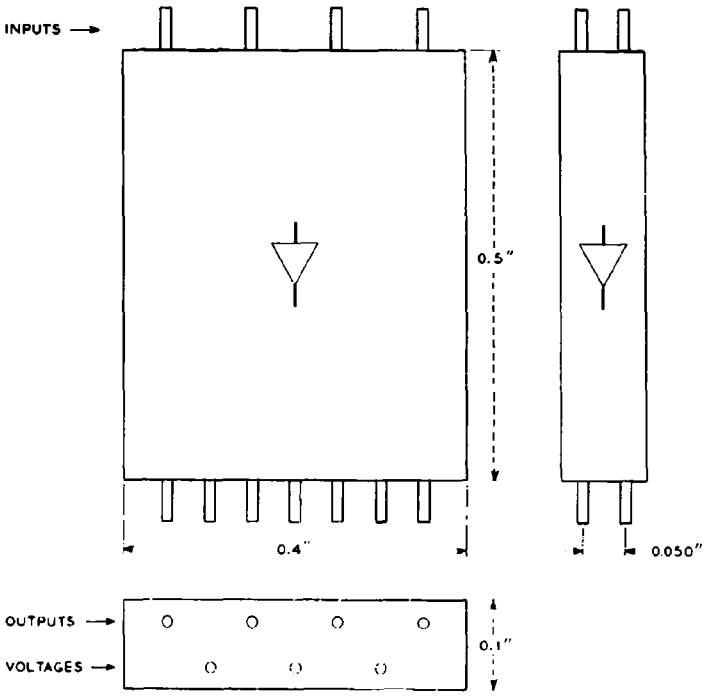


Fig. 30 - Gate package for three-dimensional design showing size and lead configuration. (Scale 5:1)

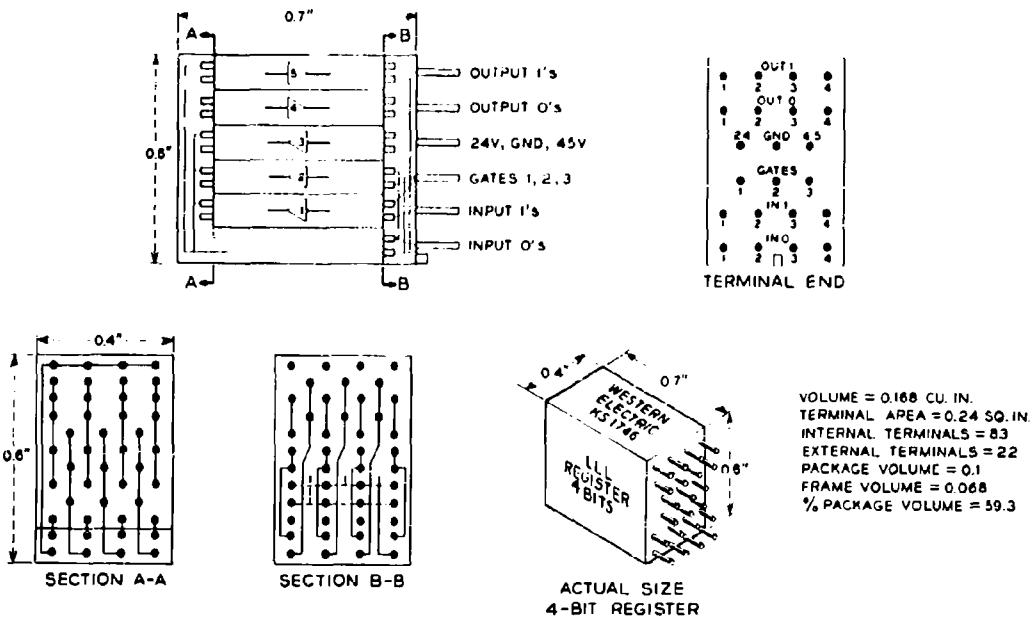


Fig. 31 - Three-dimensional design for 4-bit register showing position of gate packages and the interconnecting frame.

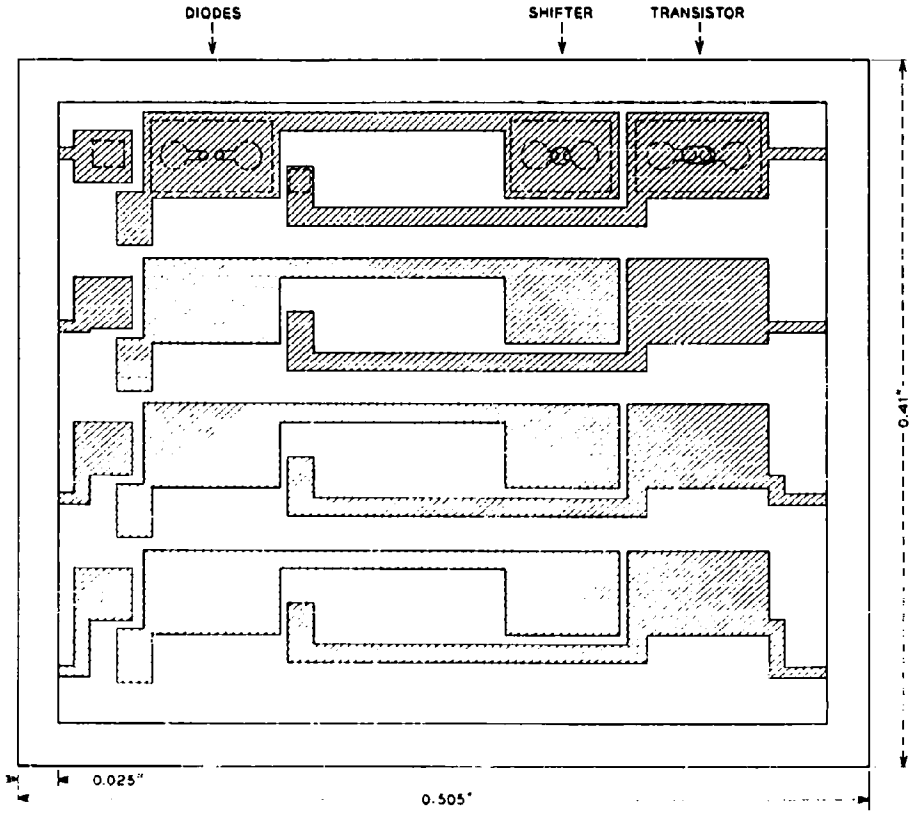
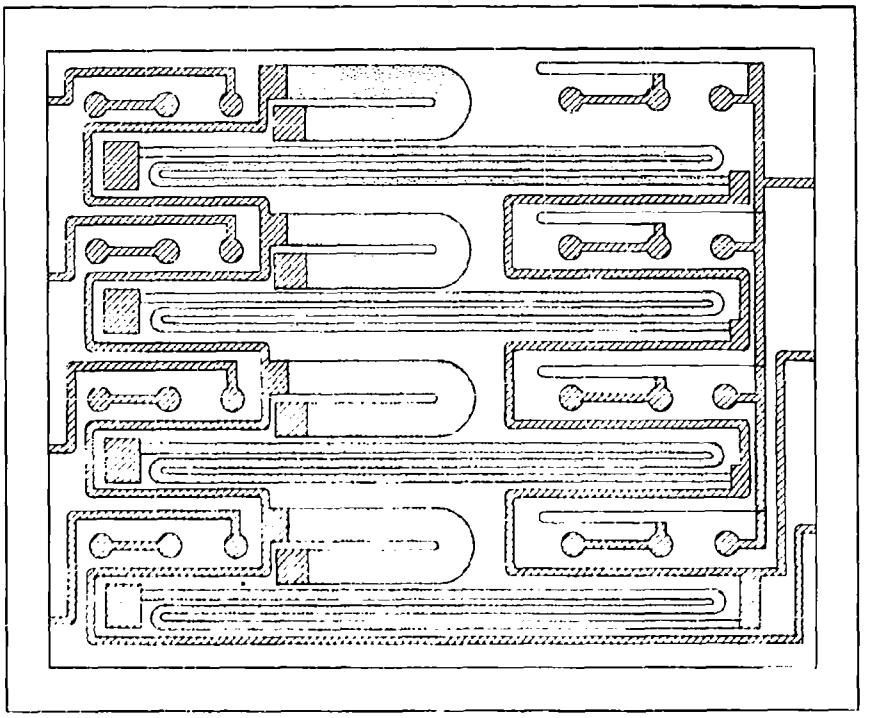


Fig. 32 - Internal arrangement of gate package showing the first layer of metallized areas and silicon chips. (Scale 10:1)

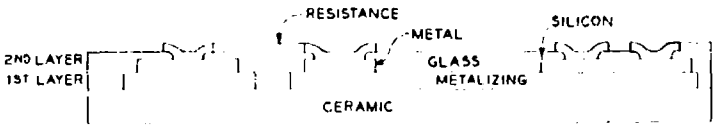
These resistors, the semiconductor chips, and the interconnections might be put on a single plane, but again it was found that the two-plane approach provided easier interconnections and also decreased size. In this case, the "third" dimension consisted of a double layer, the first containing the semiconductor chips and the second the resistors, with connecting strips on both planes. The design is shown in Figs. 32 and 33. The process would typically involve three steps: metallize ceramic, bond semiconductor chips, mold glass-fill leaving appropriate openings, deposit resistive-metal and conductive-metal, and etch pattern.

The construction of the package can be done in several ways. If made from ceramic as in Fig. 34, the leads connecting to the terminals might be metallized on the ceramic as well as on the circuit pattern.

The frame of the bit package could also be ceramic. All of the interconnections on the "L" shaped piece would be printed wire. If the shape causes difficulty in the development of the pattern, this section could be divided in two with appropriate connections inserted. The connections are shown as plug receptacles so that the gate packages might easily be inserted and removed. The connections might also be holes in which the package terminals would be soldered. The terminal piece also has some printed wiring, but also necessarily some wire connections molded in to



(a)



(b)

Fig. 33 - Internal arrangement of gate packages (Scale 10:1)
(a) Second layer of resistive and conductive metal strips.
(b) Cross section showing the glass insulating layer.

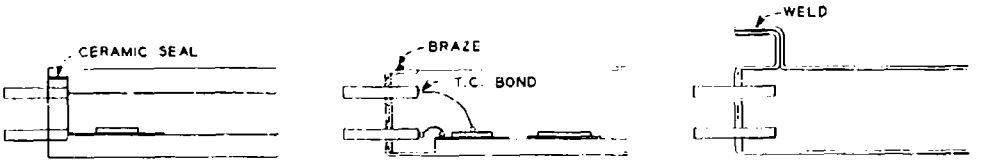


Fig. 34 - Possible gate package construction (Scale 5:1)
(a) Ceramic package. (b) Kovar-glass package with braze.
(c) Kovar-glass package with weld.

connect to the bit-package terminals. Plug receptacles are used in this piece as no alternative seems apparent.

Thus, the individual packages appear feasible, as does the frame used for interconnecting and the over-all arrangement appears to offer some considerable advantages which will be considered in more detail in the next section.

4.4 COMPARISON OF RELEVANT STATISTICS

To obtain a better comparison of the various integration techniques, the relevant statistics which result will be considered in this section. The various aspects included in the relevant statistics shown in Table 4-1 all affect the cost, reliability and size of the subfunction and hence the system.

TABLE 4-1

Integration Techniques	No. of Package Types		No. of Packages		No. of Leads	Layout Area (Sq. In.)	Equipment Volume (Cu. In.)
	SC	Res.	SC	Res.			
Conventional	3	3	480	336	1752	375	140
S-C T05	2	3	90	336	1422	166	62
S-C Ceramic	3	3	90	336	1542	148	60
S-C+R T05	2	1	84	108	972	164	62
S-C+R Ceramic	1	-	30	-	498	-	1

The first aspect listed is the number of package types and it can be seen that in no case is this number excessive. Greater differences can be seen in the next column referring to the total number of packages necessary. Both of the integration techniques using the printed-circuit board and integrating only the semiconductor devices lead to essentially the same gain of about a factor of 5 over the conventional case. With the incorporation of the resistors into the integrated package there is a further gain of about a factor of 3 for the passive components. The greatest gain is made in the last case, arising from the double-plane ceramic package which can contain a larger number of devices.

The next aspect to consider is the total number of package leads, which also reflect the number of connections, or soldered joints, which must be made. This in turn affects the reliability of system. It can be seen, for this particular case, that appreciable inroads into the interconnection problem are only made when both semiconductor devices and resistors are integrated. In these cases the gain lies, approximately, between a factor of two and a factor of 4.

The last two columns reflect the size reduction which is achieved. The gain is restricted to about a factor of 2 as long as printed-circuit boards are used. However, when we consider the last case we find a dramatic reduction of a factor of 140 even though the decrease in number of packages is only a factor of 16.

The reason for this gain may be stated generally as being due to the fact that the problem of integrated package design and the next stage of equipment design was considered as a whole. Consequently, the dimensions and lead arrangement of the packages and the dimensions and interconnection system of the frame were jointly optimized. This extra degree of freedom, added to the assumption of smaller film wiring in the frame, leads to the extremely compact equipment design.

4.5 CONCLUSIONS

The various techniques of integrating the register may be considered as representing several stages in evolution of integrated circuit technology.

1. The first stage involves the simple integration of like components (e.g., semiconductor devices) within a single encapsulation with subsequent assembly on standard circuit boards. Here we have considered two cases, a standard T05 encapsulation and a more sophisticated ceramic package. The gains are substantial and essentially the same in both cases. Showing that this approach is a good starting point and that sophisticated packaging is not essential as long as the packages must be compatible with existing equipment techniques (circuit boards).

2. The second stage involves the simple integration of unlike components (active and passive) within a single encapsulation with subsequent assembly on standard circuit boards. In this case we obtain a greater gain in the interconnection problem and in the over-all number of packages but little further decrease in size. Nevertheless, this study indicates that it is desirable to achieve the common integration of active and passive components.

3. The third stage consists of more complex integration with larger numbers of unlike components in more sophisticated packages which are designed to facilitate improvements in the next stage of equipment design. Here, the removal of the restriction of the standard printed-circuit board allows further gains across the board but particularly dramatic is the case of the decrease in size. The particular conclusion to be drawn is that the greatest gains in interconnection and size are made when the integrated packages and the equipment design are optimized together, rather than considered separately.

In summary, the studies have shown that the basic concept of integrating through the use of multiple device chips in a single encapsulation is compatible with an evolutionary program to develop integrated circuit technology. Further, the examples have shown the order of the gains which may be made in the various stages of evolution and that it is important to develop the circuit equipment and the integrated packages simultaneously in a compatible fashion.

REFERENCES

1. M. M. Atalla, Report No. 5 on Transistors, Contract DA 36-039 sc-88962 3 August 1961, Chapter 3.

2. C. J. Spector, W. H. Jackson, Tantalum Film Circuits, Proceedings of Electronic Components Conference, May 1961.

Chapter 5

AN INTEGRATED SYSTEM CLOCK

By B. T. Howard, R. Lindner, D. A. Naymik and G. Reich

5.1 INTRODUCTION

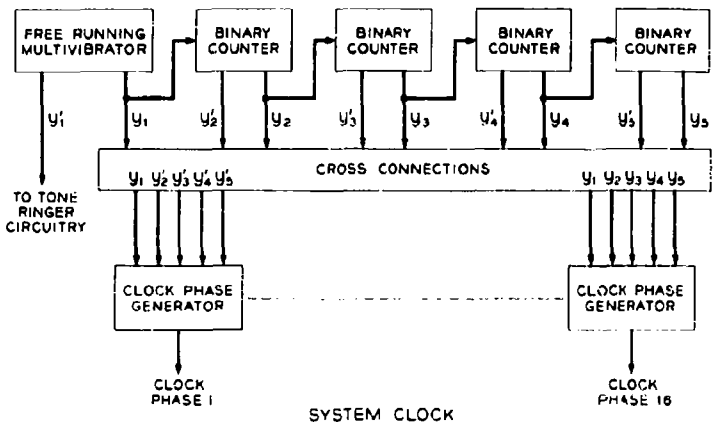
Integration of a system function has been completed in the last interval. The basic procedure of the method of integration, i.e., the package design and printed-board layout, has been discussed in Chapter 3 of this report. This chapter is concerned with the actual packages and boards produced, their design, and final characteristics.

The function chosen to be implemented was a system clock, which is shown in Fig. 35. The clock is designed to produce a one-millisecond pulse in sequence at each of sixteen outputs, each separated in time by a millisecond. This is done by taking the coded outputs from a free-running multivibrator and four binary counters, and feeding these to sixteen five-input gates with pulse-forming amplifiers. The pulse forms are shown in Fig. 36.

5.2 COMPONENTS TO BE INTEGRATED

The clock phase-generator circuit of Fig. 35 contains a PNP transistor with a click reducer. Since at this time a planar silicon PNP transistor was not readily available, it was decided not to integrate the PNP transistor or the click reducer. The NPN transistors, P^+N diodes and N^+P diodes are integrated in T05 header assemblies with eight leads. The devices are arranged in functional groups since this led to the minimum number of packages. It was also decided to integrate the passive components separately, using thin tantalum films (Ref. 1) on glass substrates (Refs. 1, 2). The fabrication of the film resistors and capacitors was done on 3" x 1" glass slides. This work was carried out by the Components Laboratory of Bell Telephone Laboratories (Ref. 2).

In the functional design, 26 NPN transistors, 98 N^+P diodes, and 8 P^+N diodes are encapsulated in 22 integrated packages. In addition, 88 resistors, and 14 capacitors are fabricated on six glass slides.



CROSS-CONNECTION TABLE

PHASE	TERMINAL CONNECTION				
	1	2	3	4	5
1	y_1	y'_2	y'_3	y'_4	y'_5
2	y_1	y_2	y'_3	y'_4	y'_5
3	y_1	y'_2	y_3	y'_4	y'_5
4	y_1	y_2	y_3	y'_4	y'_5
5	y_1	y'_2	y'_3	y_4	y'_5
6	y_1	y_2	y'_3	y_4	y'_5
7	y_1	y'_2	y_3	y_4	y'_5
8	y_1	y_2	y_3	y_4	y'_5
9	y_1	y'_2	y'_3	y'_4	y_5
10	y_1	y_2	y'_3	y'_4	y_5
11	y_1	y'_2	y_3	y'_4	y_5
12	y_1	y_2	y_3	y'_4	y_5
13	y_1	y'_2	y'_3	y_4	y_5
14	y_1	y_2	y'_3	y_4	y_5
15	y_1	y'_2	y_3	y_4	y_5
16	y_1	y_2	y_3	y_4	y_5

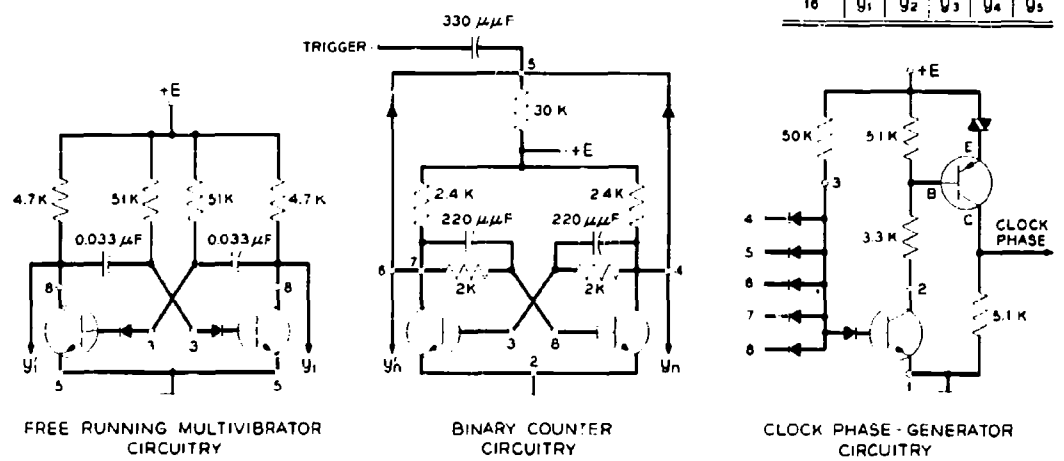


Fig. 35 - Schematic circuit of system clock and the repeated circuit blocks with the cross connection table.

5.3 CONNECTION OF PACKAGES INTO BOARDS

Insertion of the leads from an eight-leaded T05 header directly into holes in a printed-wire board does not provide enough space for the solder lands. Therefore, the wires have to be bent out into a larger circle. It was felt that this could be accomplished with a more rigid structure by inserting the can into the board with the leads bent back as shown in Fig. 37. The film glasses molded in a plastic frame are also connected in a similar manner, except that the many soldered connections were used as the mechanical support.

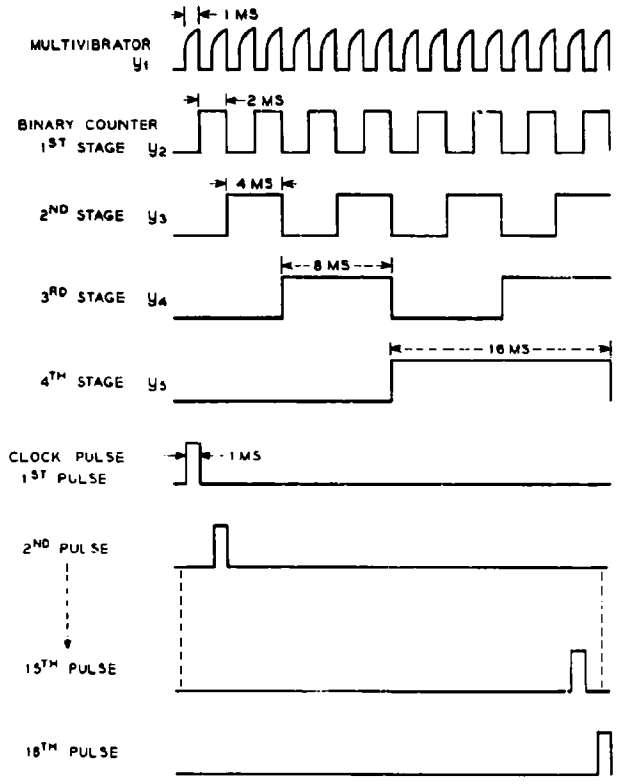


Fig. 36 - Schematic representation of the waveforms of the multivibrator, binary counter, and clock phase-generator outputs.

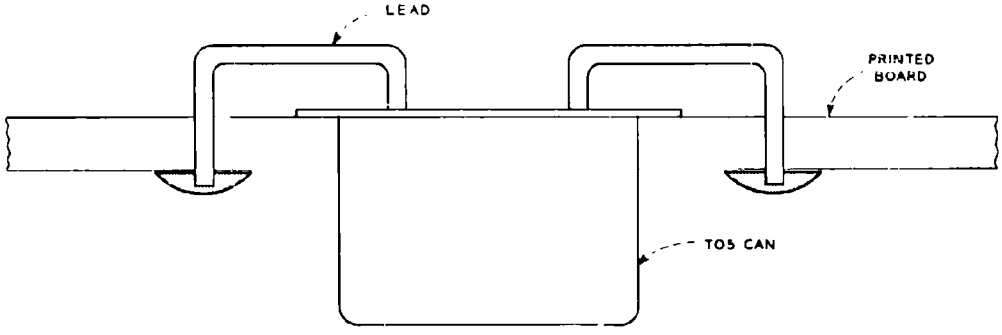


Fig. 37 - Method of inserting can and leads into printed-wire board.

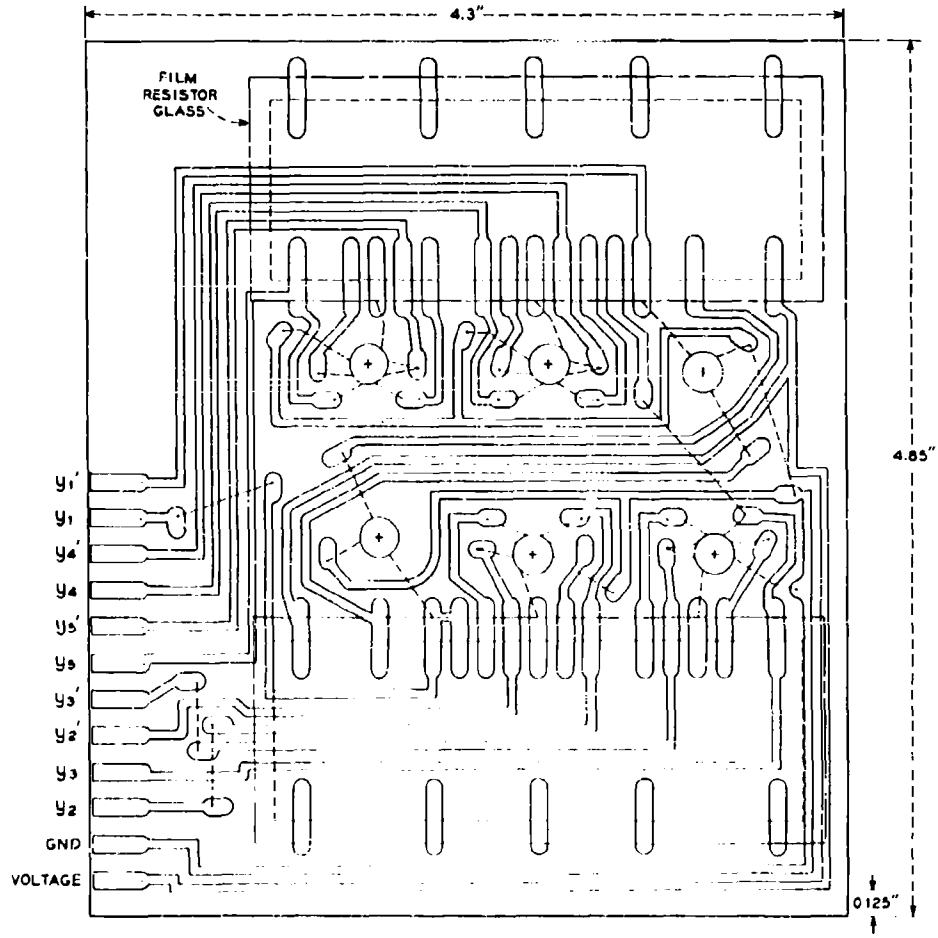


Fig. 38 - Layout plan of multivibrator and binary counters on printed-wire board showing position of integrated packages and tantalum film packages.

5.4 DESIGN OF BOARDS

The layout arrangement of the clock was split into a group of standard printed-wire boards. The printed boards are single-sided and used jumpers on the back where crossovers are necessary. The first board contained the multivibrator and the four binary counters. Six integrated packages and two film slides were required. The layout design requiring the least area is shown in Fig. 38. It is 4.85" wide by 4.3" long. The sixteen clock phase-generator circuits were split into four identical boards, each containing four such circuits. Each board requires four integrated packages, one film slide, and four PNP germanium alloy transistors and associated click reducers. The clock phase-generator board is shown in Fig. 39. It is 3.95" wide by 4.3" long. The eight jumpers which were used are concerned with the cross connecting pattern of Fig. 35 to provide the correct binary counter output to the gate inputs.

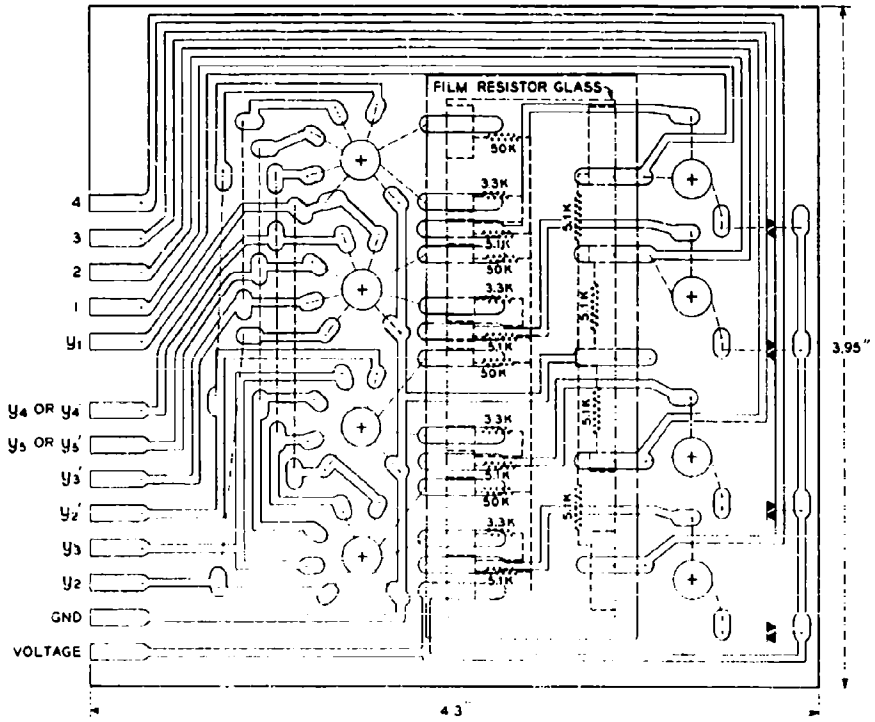


Fig. 39 - Layout plan of four clock phase-generator circuits on printed-wire board showing position of integrated packages, PNP transistor, click reducer, and the tantalum film package.

These five boards are assembled into the finished clock by the addition of a sixth board, the terminal board. This board, shown in Fig. 40, completes the cross connecting pattern, provides the voltage inputs, and provides for the eighteen outputs. The five circuit boards are connected, end-on, to the terminal board by means of short wires. The complete structure is shown in Fig. 41. Note that the terminals for voltage, ground, and the binary-counter outputs y_2, y_3, y_2', y_3' are in the same relative position on each board enabling a simple straight line connection to be used on the terminal board. The connections of y_4, y_4', y_5, and y_5' are different for each clock phase board and it is this which determines which group of clock phase outputs (1-4, 5-8, 9-12, or 13-16) is contained on each board.

The construction of the cabinet into which the clock was to be inserted dictated some of the spacings which were used. The boundary conditions were that the external terminals had to be 18-mil phosphor-bronze wires on 100-mil centers and the spacing between boards had to be 0.5-inch. Maintaining the 0.5-inch separation required that 1/8-inch thick washers be fitted on the cans as shims to prevent complete insertion into the board.

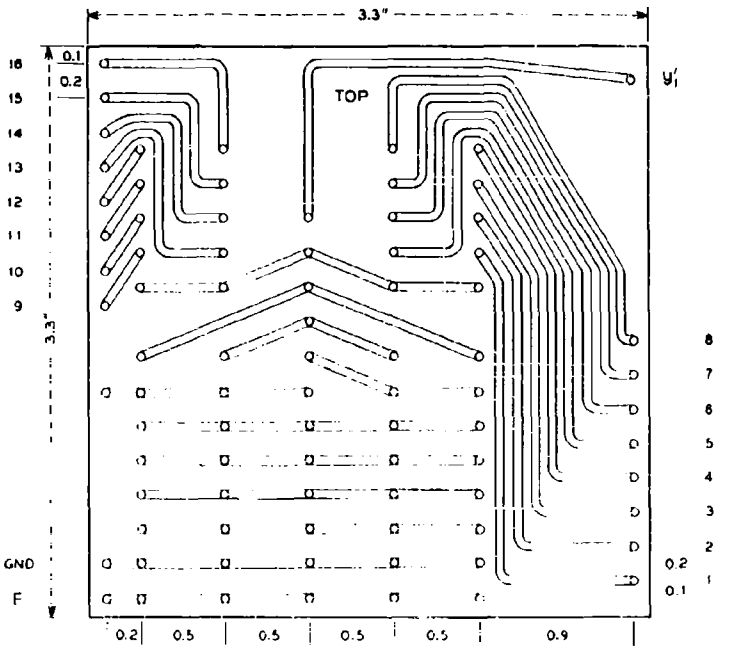


Fig. 40 - Layout plan of terminal board providing connections between the element boards.

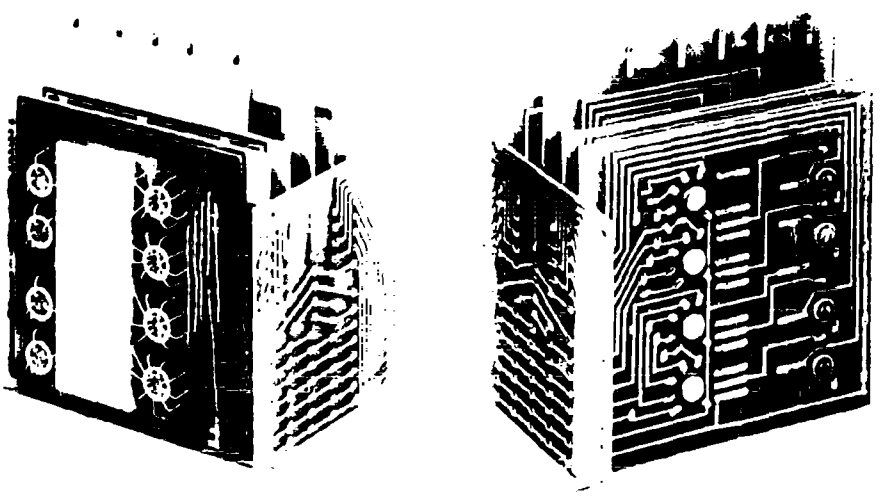


Fig. 41 - Complete assembly of integrated system clock.

5.5 DESIGN OF PACKAGES

The device grouping and allocation of leads were determined from the analysis reported in Chapter 3 and from the printed board layouts. The general construction consists of using chips of silicon containing planar diodes or transistors and bonding them to the platform or pins. Thermal compression bonding of 0.7-mil gold wire to the contact areas and pins complete the electrical continuity. The diode chips all contained six separate diffused areas, but as few as one of these might be used in a package. The transistor chips all contained a single transistor.

The three types of packages made are the multivibrator package containing one N^+P diode and one transistor, the binary counter package containing two P^+N diodes and two transistors, and the clock phase package containing six N^+P diodes and one transistor. The circuits and layouts for these packages are shown in Fig. 42. For a complete clock it was necessary to make two multivibrator packages, four binary-counter packages, and sixteen clock phase packages. A total of 132 transistors and diodes are contained in these 22 packages for a 6 to 1 reduction in the numbers of packages.

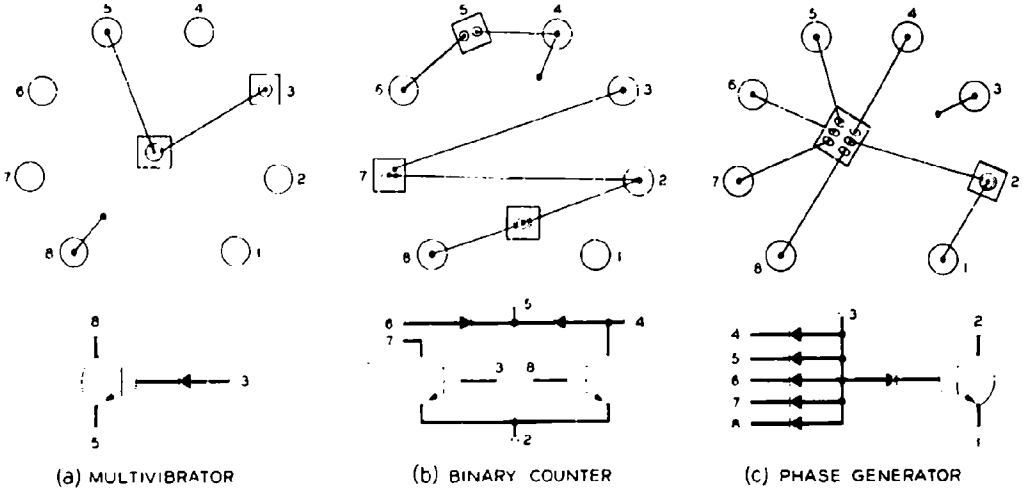


Fig. 42 - Internal package design showing position of silicon chips and interconnecting wires.

Another method of fabrication which has also been used is to provide a ceramic insulator bonded to the platform of the header. On the ceramic a pattern of metallized areas is provided, to which chips or wires can be bonded. This structure eliminates the need to bond directly to the top of a pin which is only 24-mils in diameter. It is also felt that the use of metallized ceramic will provide a more versatile means of obtaining the connections between contact areas and silicon bodies. The same three packages using ceramic insulators are shown in Fig. 43. This type of package has been made and is electrically identical to the pin-mounted type. However, the units used in the fabricated clock of Fig. 41 use only the pin-mounted packages.

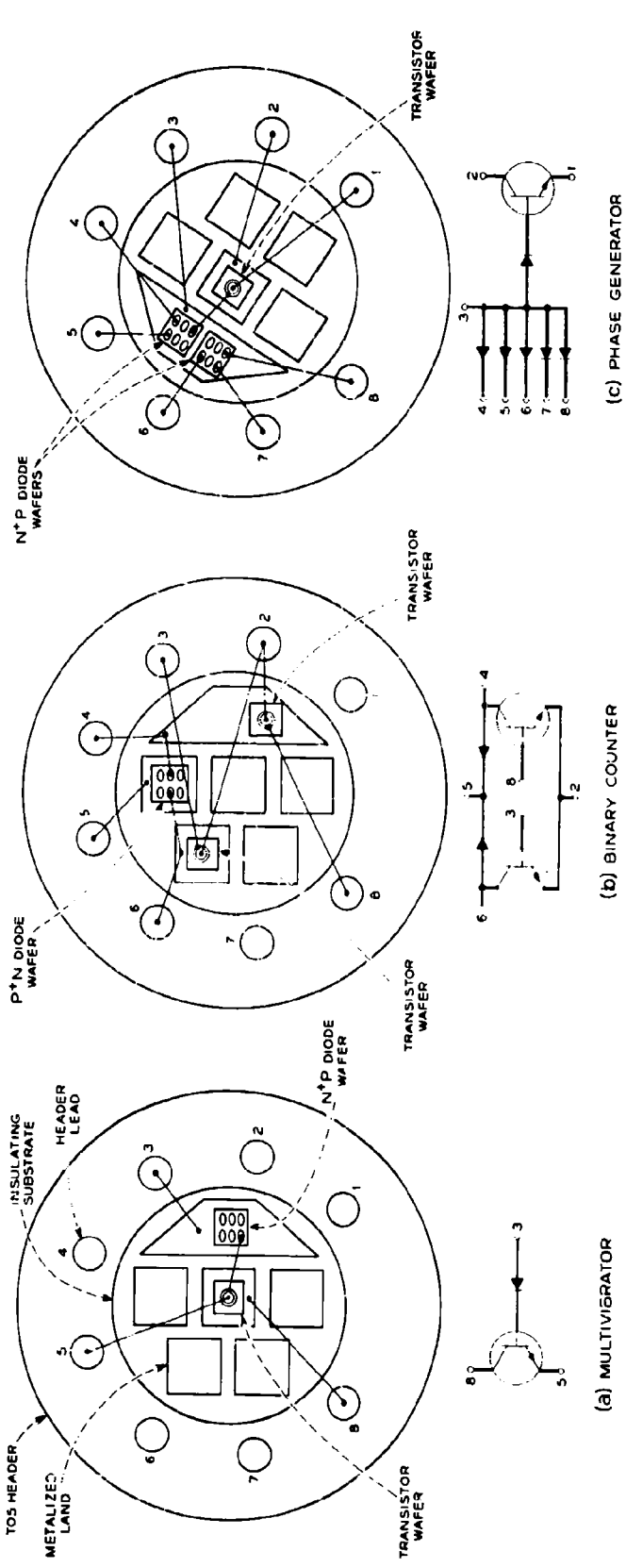


Fig. 43 - Internal package design using metallized ceramic wafers bonded to header platform.

5.6 WAFER PROCESSES

Three types of wafers were fabricated, the P^+N diodes, the N^+P diodes, and the NPN transistors. The diodes were oval shaped 4.5 mil x 3.5 mil and were fabricated in groups of six which are on 30-mil centers. The transistor has a 10-mil diameter base and a 4-mil diameter emitter and uses a "ring-dot" contact.

All were fabricated using limited diffusion or planar technology. For the diodes the slice was oxidized, photoresisted, diffused, gold-diffused, photoresisted for contacts, and aluminum contacts applied. For the transistor the additional steps for photoresisting and diffusing the emitter were added. Finally the wafers were broken into 30-mil chips.

5.7 WAFER CHARACTERISTICS

The P^+N and N^+P diodes were made to the specifications of the 1N696 computer diode, which has a breakdown voltage of > 40 volts, and a storage time of < 5 nanoseconds. In the case of the N^+P diodes, a breakdown voltage of 35 volts was regarded as acceptable. The low storage time of the 1N696 is not necessary for the system clock but demonstrated capability for other subfunctions.

The transistor is the planar equivalent of the 2N560 silicon-diffused-mesa NPN whose specifications are $\alpha = 0.97$, total switching times = < 100 nanoseconds, measured as shown in MIL-S-19500B, and cutoff frequency $f_T = 50$ mc. In addition it was required that BV_{CE} sustain be at least 30 volts.

5.8 PACKAGE CHARACTERISTICS

The packages were characterized both by measuring individual devices as far as was possible and by operation in the system clock circuit. In the case of the multivibrator, Fig. 42(a), the quantities measured and typical values are given in Table 5-1.

TABLE 5-1

V_{CEO} Collector to Emitter Voltage, $I_c = 50\ \mu a$, $I_B = 0$	50 volts
I_{CEO} Collector to Emitter Current, $V_{CE} = 25$ V	0.003 μamp
V_{EBO} Emitter to Base Voltage	7 volts
Diode Breakdown Voltage + Emitter Breakdown Voltage	65 volts
Diode to Emitter Current, V = 25 V	0.001 μamp
Forward Voltage - Diode to Emitter, I = 10 ma	1.5 volts
h_{FE} DC Current Gain, $I_c = 0.5$ ma, $V_{CE} = 4.5$V	60

Note that the diode characteristic can only be measured with the emitter in series.

TABLE 5-2

V_{CEO} Collector to Emitter Voltage, I_c = 50 μa, I_B = 0	50 volts
I_{CEO} Collector to Emitter Current, V_{CE} = 25V	0.003 μamp
V_{EBO} Emitter to Base Voltage	7 volts
V_F Collector to Base Voltage, I_{BC} = 10 ma	0.75 volts
h_{FE} DC Current Gain, I_c = 0.5 ma, V_{CE} = 45V	60
V_B of Diode, I = 50 μa	60 volts
I_R of Diode, V = 25V	0.003 μamp
V_F of Diode, I = 10 ma	0.75 volts

In the case of the binary counter, Fig. 42(b), the two transistors and two diodes can be measured separately and give typical values for the transistor and P^+N diode as shown in Table 5-2.

Each device of the clock phase-generator package, Fig. 42(c), can be measured separately except that of the diode in the base lead of the transistor which must be measured in series with the emitter. Another measurement (between diodes) must be made to insure that a channel or inversion layer does not exist between the diffused areas associated with each diode.

The final check of each package was to operate it under circuit conditions for at least 90 hours before it was incorporated into the printed-wire boards.

5.9 CLOCK CHARACTERISTICS

The finished clock of Fig. 41 has the same characteristics as the original non-integrated clock. The waveforms produced by the multivibrator, binary counters, and clock phase-generators conform to the system specifications. The multivibrator pulse is 1.1 milliseconds which is 10% above the nominal value. This may be due to the higher resistor or capacitor values associated with the multivibrator. Fig. 44 shows the waveforms of the multivibrator, 1.1 ms pulse; the first binary counter, 2.2 ms pulse; the secondary binary counter, 4.3 ms pulse; the third binary counter, 8.6 ms pulse; and the fourth binary counter, 17.2 ms pulse. The fourth binary-counter pulse is shown for comparison with each of the others.

In Fig. 45 each of the 1.1 millisecond pulses from each of the clock phase outputs is shown in its relative position in time compared to the output of the fourth binary counter. Note that each pulse is separated in time by a time equal to a pulse width so the complete cycle of 16 outputs takes 34 milliseconds.

This system clock has been operated for approximately 100 hours without difficulties of any kind.

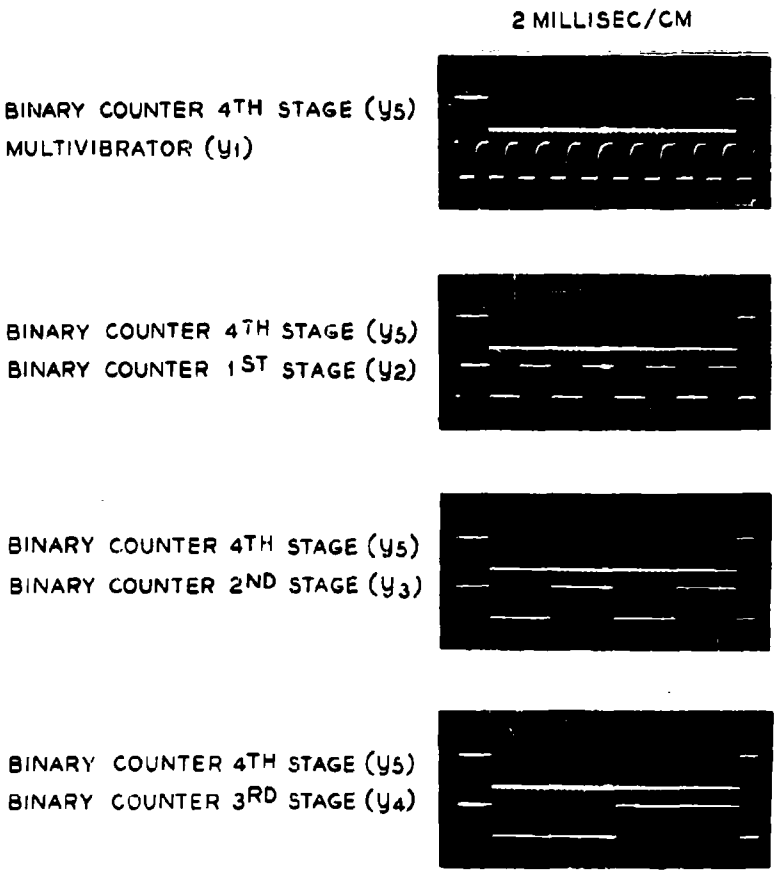


Fig. 44 - Output waveforms of multivibrator and binary counters.

5.10 SUMMARY

A complete system subfunction has been integrated using packages containing particular groups of devices as well as tantalum film resistors and capacitors. The system performs the function of a clock producing one-millisecond pulses at intervals of one millisecond at each of 16 outputs.

The packages required were of the functional type using for the three types:

1. Multivibrator - 1 2N560 and 1 1N696 - 2 required
2. Binary counter - 2 2N560 and 2 1N696 - 4 required
3. Clock phase-generator - 1 2N560 and 6 1N696 - 16 required

A total of 132 transistors and diodes are contained in these 22 packages for a 6 to 1 reduction in the numbers of packages.

The clock was integrated using a total of six printed-wire boards. Four are used for four each of the clock phase-generator circuits, one for the multivibrator

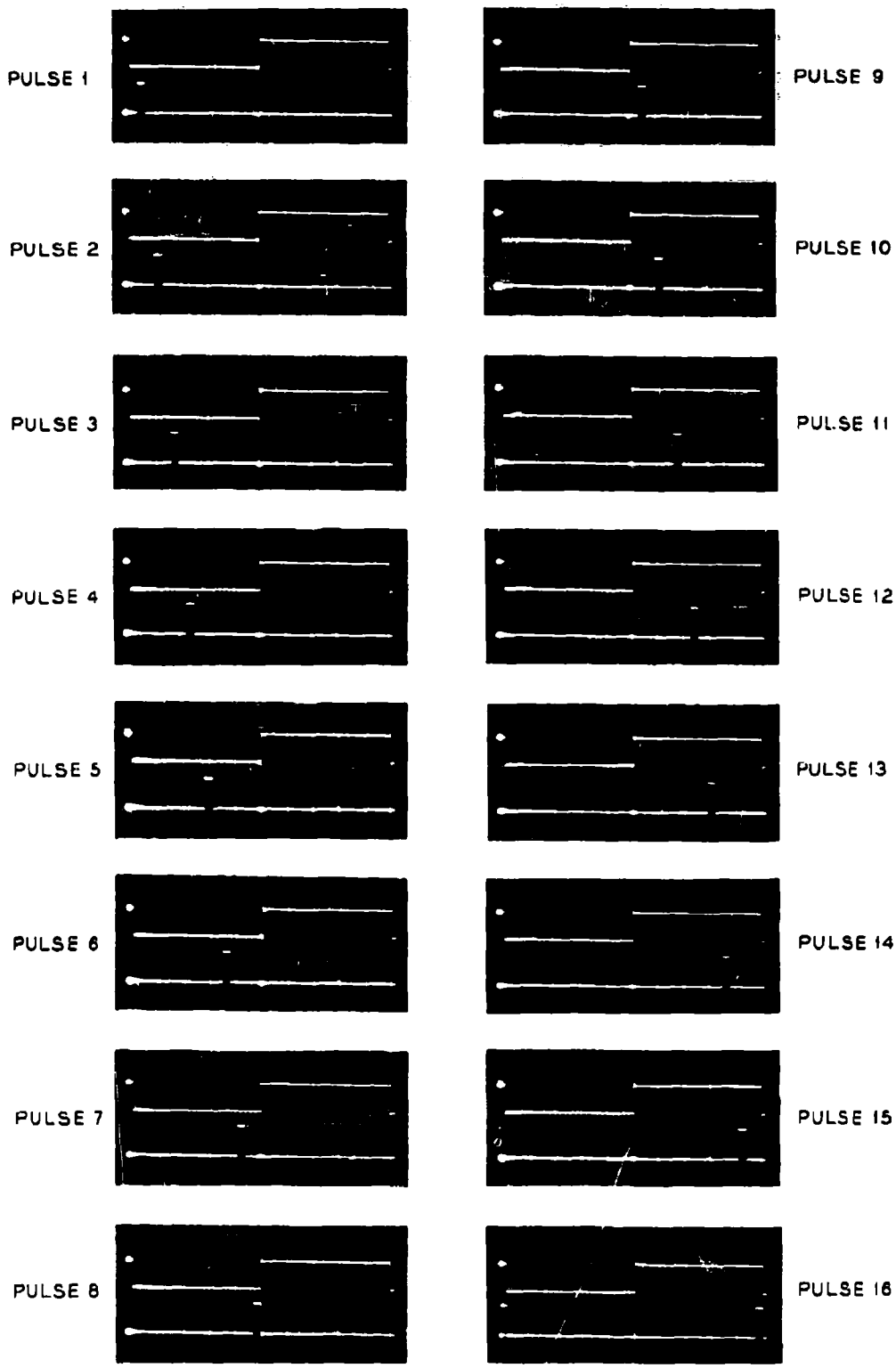


Fig. 45 - Output waveforms of completed integrated system clock. Upper traces are the fourth binary-counter output and bottom traces are outputs of the sixteen clock pulse-generators.

and binary counters, and the last as a terminal board which connects the other five. The entire structure is 4.8 inches high, 4.3 inches deep, and 3.3 inches wide.

The packaging of several devices in a small volume has not affected the electrical performance of the circuit. The waveforms at each terminal have been recorded during operation and found to be correct. The clock has, thus far, operated for about 100 hours without difficulty.

REFERENCES

1. C. J. Spector and W. H. Jackson - "Tantalum Film Circuits," Proceedings of Electronic Components Conference, May 1961.

2. D. A. McLean, R. W. Berry and C. J. Spector - This work was not supported by the contract.

SECTION 5 - CONCLUSIONS

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

The use of an oxide for the separation of the emitter and base electrodes in the planar transistor structure requires refined evaporation techniques. Scattering of the oxide onto the germanium surface during the evaporation results in erratic alloying of the electrodes. This effect can be minimized by proper evaporation techniques. Planar devices of the desired structure can be made, but additional process development is necessary before the transistors will meet the objectives.

Noise figure calculations for the M2275 indicate a noise figure of less than 5 db should be obtainable in amplifiers with adequate gain and stability.

Investigation of the power gain of some mesa transistors has revealed a probable cause of the abnormally low 1-kmc power gain observed in some of these units. The low Q of that part of the output capacitance lying between the base stripes and mesa edge resistively loads the output of the device. This result further indicates the need for heavy base doping, close mechanical tolerances in the structure, and the advantage of the planar structure.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Studies of the effect of the use of different classes of integrated circuit packages on circuit-board layout have demonstrated the need for flexible technology. The optimum circumstances were defined as those which minimized the size of the layout, the number of package types, the total number of packages and the number of leads. It was found, with the use of these criteria, that the packaging technique should be flexible enough to allow the fabrication of multiple-like devices, logic gates and hybrid arrangements if layout optimization is desired.

One technique which allows this flexibility of grouping is the encapsulation of several semiconductor-device chips in a single package. Studies of the use of this technique for the integration of a 24-bit register have shown that it is compatible with an evolutionary program to develop integrated circuit technology.

This technique has been successfully reduced to practice for the case of a system clock. This example has demonstrated that considerable gains may currently be achieved through the use of the concept of common encapsulation of multiple-semiconductor-device chips.

SECTION 6 - PROGRAM FOR THE NEXT INTERVAL

TASK 4 - NEW AND IMPROVED TRANSMISSION TYPE TRANSISTORS

Processing studies will be continued so that devices meeting the M2260 and M2275 objectives can be met. Electrical evaluation and design analysis will also continue.

TASK 9 - FUNCTIONAL DEVICES AND INTEGRATED CIRCUITS

Studies of the evaluation of alternative methods of various subsystem functions will continue. An objective of this program is to determine general rules for optimization of layout for applicability to various classes of subsystem functions.

Work on the integration of specific subsystems functions will continue.

Development of technology for use in integrated circuit fabrication will continue.

SECTION 7 - IDENTIFICATION OF PERSONNEL

GEORGE REICH

George Reich attended C.C.N.Y. and RCA Institute. He served in the U.S. Army during the Korean conflict as an instructor in Nike Ajax Guidance Systems. He joined Bell Telephone Laboratories in 1953 and is presently engaged in semiconductor device development.

Earlier reports under this contract and its predecessor contracts have identified other engineers and scientists whose work has contributed materially to this program.

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Third Quarterly Report, 31 May 1962
Period, 1 January to 31 March 1962
Contract DA 36-039 sc-88931 (Unclassified)

Prepared by: R. E. Davis, A. G. Foyt, B. T. Howard, R. Lindner, D. A. Naymik, G. Reich

Report No. 8, 72 pp, incl. 45 illus, 8 tables

The general objective of this contract is to make studies and investigations related to transistors and transistor-like devices, with a view toward demonstrating and increasing the practicability of their use in operating equipment.

This report covers the status of work on microwave germanium transistors and on integrated circuit devices.

Problems of oxide scattering during fabrication of the proposed oxide-spaced planar structures of the M2260 and M2275 germanium microwave transistors are discussed. Noise figure calculations for the M2275 (low power, 3Gc) indicate a noise figure of less than 5 db at 1Gc as a reasonable value. Models of the M2260 (1-watt, 1Gc) have been fabricated and show transistor action with a common-emitter current gain of 8. High frequency y-parameter measurements on 3-stripe mesa units with 1 by 20 mil stripes showed abnormally high values of g22. This effect is thought to be due to the resistance in series with that part of the collector capacitance not directly under the base electrodes. The oxide-spaced structure should alleviate this problem.

Studies to evaluate alternate methods of integrating circuits and subsystems functions are discussed. It is found that the packaging technique used should be flexible enough to permit the fabrication of multiple-like devices, logic gates, and hybrid arrangements if layout optimization is to be achieved. The design and fabrication of a system clock which illustrates the results achieved from the concept of common encapsulation of multiple semiconductor chips is described.

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Studies to evaluate alternate methods of integrating circuits and subsystems functions are discussed. It is found that the packaging technique used should be flexible enough to permit the fabrication of multiple-like devices, logic gates, and hybrid arrangements if layout optimization is to be achieved. The design and fabrication of a system clock which illustrates the results achieved from the concept of common encapsulation of multiple semiconductor chips is described.

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Prepared by: R. E. Davis, B. T. Howard, D. A. Naymik, A. G. Foyt, R. Lindner, G. Reich

Report No. 8, 72 pp, incl. 45 illus, 8 tables

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